VERY HIGH SPEED INTEGRATED CIRCUITS

-VHSIC-

ANNUAL REPORT FOR 1988

VHSIC PROGRAM OFFICE

OFFICE OF THE UNDER SECRETARY OF DEFENSE FOR ACQUISITION

31 December 1988

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DECEMBER 31, 1988

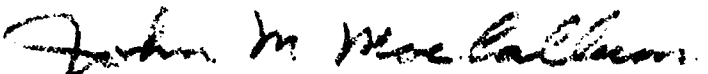
FOREWORD

This report presents the accomplishments made during the eighth year of the VHSIC program. New technology achievements have been made and new VHSIC products have found their way into the defense industrial base market. Accomplishments in technology insertion (both VHSIC funded efforts and independent insertion projects), design tool development, device qualification and testing, submicron technology, lithography, radiation hardening, packaging, interoperability, and training are presented in this report.

Over the past several years, the VHSIC program has evolved from a program focused on developing advanced military integrated circuits to one which involves a full spectrum, "concept-to-system", capability that is available to satisfy our demanding national security requirements. The program is involved with developing new materials, new design tools, advanced processes, new manufacturing equipment, new qualification requirements and procedures, new levels of radiation hardening, new data interface standards and specifications, and improved techniques for built-in-test and maintainability. All of these efforts are aimed at supporting a framework for system design that exploits advanced technology. The aggressive challenge initially laid down by the VHSIC program has been picked up by a majority of the semiconductor industry. Companies who were not part of the VHSIC program take great pride in announcing that they have met or, in some cases, even exceeded VHSIC goals. Companies all over the country are requesting copies of the VHSIC data interface standards and specifications. Our achievements in test structure development and definition of new qualification procedures has evolved into a new DoD initiative to establish Qualified Manufacturing Lines. Our VHSIC Hardware Description Language has been adopted as an international standard. Fundamental knowledge in design, processing and testing developed on the VHSIC program is migrating into commercial production lines and is contributing to maintaining our national technical leadership. And finally, VHSIC technology and products are starting to appear in a wide variety of weapon system development programs. In addition to those funded through the VHSIC technology insertion program, we have identified over 60 different independent insertion efforts. As these systems proceed into production and eventually into the field/fleet, we will begin to experience the tremendous impact of VHSIC technology on our weapon system capability.

Many other technical accomplishments are included in this report. Several have taken on 'lives' of their own; becoming part of company operating procedures or providing the seed for

technology growth in new areas. Some are not yet complete such as the Engineering Information System and actual demonstrations of the 0.5 micron capability. Our challenge over the next and last year of the VHSIC program is to complete our ongoing efforts, transition technology insertion responsibilities to the users, establish mechanisms to maintain standards and set the stage for new efforts that will assure we maintain our technical excellence in this dynamic, competitive, defense critical area.



John M. MacCallum
Director, Electronic Systems

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CHAPTER 1

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CHAPTER 1 - SUMMARY

Very High Speed Integrated Circuits (VHSIC) is the name of the Department of Defense program to develop two new generations of the silicon integrated circuits which are needed to provide higher performance electronics for DoD weapon systems.

1.1 BACKGROUND

The defense posture of the United States is increasingly based upon the concept of military weapon systems that are technologically superior to any potential adversary. Technology is expected, wherever possible, to leverage our ability to defend against numerically greater forces. The silicon integrated circuit, which is the basic device for processing signals in any modern electronic system, has become one of the most effective force multipliers for our Nation's defense. The technology for making the device is a very demanding one. Complex and expensive equipments are required to produce it, advanced skills and knowledge are required to use it, and large continuing, investments are required to keep it up-to-date.

The United States pioneered the introduction of the integrated circuit industry and, although we still retain a very strong position in the development and application of new products, our position in the total world production and sale of integrated circuit products has been overtaken by Japan in recent years. Are the full capabilities of our future military weapons in jeopardy? In order to ensure that those capabilities are available when we need them for our future defense, it has been deemed necessary to restore a more demonstrable lead in the early deployment of silicon integrated circuit technology.

Additional background information on the origins and previous progress of the VHSIC programs can be found in the VHSIC Annual Reports for 1986 and 1987 (references 1.1 and 1.2) and in references 1.3 through 1.10.

1.2 PROGRAM OBJECTIVES AND STRUCTURE

The specific goals of the VHSIC program are to develop an advanced semiconductor technology for military use and to sharply reduce the delay experienced by the DoD in getting that technology into systems. The VHSIC program has therefore placed a high priority on developing and maintaining a capability within the U.S. semiconductor industry to provide the products of the VHSIC program on a continuing basis such that they meet at least the following criteria:

- o be available at least as soon as comparable commercial products,
- o have lower projected life cycle cost than current technologies,

- o have higher reliability for the same function,
- o be producible to military standards and specifications,
- o have a short design/fabrication cycle time, and
- o be well documented in a way that facilitates maintenance and upgrading.

The program activities taken to reach the goals are shown in the VHSIC Road Map in Figure 1.1, and are divided into the following major areas.

- o Phase 0: Begun in March 1980 with nine contractors to define the detailed technical approaches to be taken. Completed.

- o Phase 1: Begun in May 1981 with six prime contractors to develop and produce VHSIC-1 silicon chips with 1.25 micron minimum feature sizes. Completed.

- o Phase 2: Begun in November 1984 with three prime contractors to develop VHSIC-2 silicon chips with 0.5 micron minimum feature size. Successfully completed in December 1988 by IBM. Continuing effort to completion scheduled by Honeywell and TRW during 1989.

- o Phase 3 and Other Supporting Efforts: Begun in 1980 with over 50 large and small contractors on a variety of specially focused efforts to support VHSIC technology. Efforts in lithography, design automation software, pilot line certification, chip qualification, and radiation hardening continued during 1988 and are scheduled into 1989.

1.3 PROGRAM HIGHLIGHTS

During 1988, the success of VHSIC technology and products in the electronic marketplace has continued in a wide variety of technical areas. Most of the highlights listed below, such as the Phase 2 accomplishments in submicron technology, are the direct result of the VHSIC program. Some of the objectives of the VHSIC program, however, are being realized in more indirect ways as the advanced ideas, techniques, and capabilities diffuse into the highly complex environment of the design and production of electronic systems. Particularly in the area of design automation tools, the traceability of the impact of VHSIC may be less obvious than in the hardware areas. The items below are a sample of the more significant 1988 accomplishments covered in the body of this report.

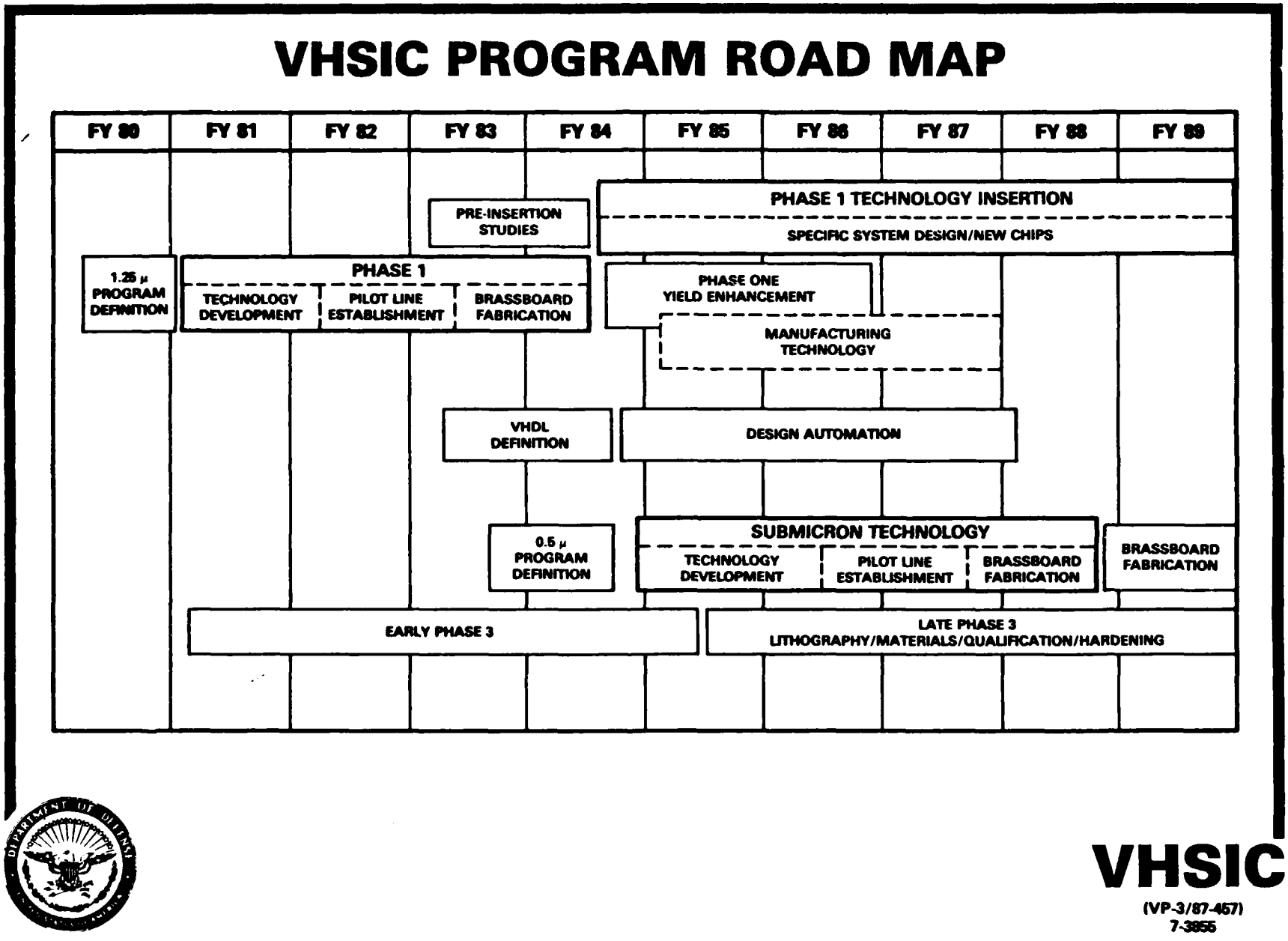

Figure 1.1 - VHSIC Program Roadmap

- The leading highlight of the year was the completion by IBM of its Phase 2 submicron development on schedule (and within budget). IBM has successfully designed and fabricated four large chips and demonstrated them in a brassboard performing sonar beamforming computations at a 50 MHz clock rate. More important from a long term point of view, IBM has convincingly shown that these large chips can be designed and manufactured at very affordable cost levels (that is, competitive with current technology). In addition, very high levels of radiation hardness are attainable in these chips at no significant increase in manufacturing complexity. (Chapter 4, Section 4.3).

- The number of companies reporting on the development of design automation tools specifically targeted for use with the VHSIC Hardware Description Language (VHDL) has increased sharply. These efforts represent a significant diffusion of VHSIC developed technology into the electronics sector of the U.S. economy, and are based on the acceptance of VHDL as a standard. Twenty-one such efforts are described in Chapter 2, Section 2.4.

- The insertion of submicron VHSIC technology into an active system development was begun by Honeywell and General Dynamics. The two submicron gate arrays being developed by Honeywell for Phase 2 are being used as the basis for the design of a Cruise Missile Advanced Guidance system. Preliminary work done by General Dynamics indicated that the guidance performance requirements could be met within the weight, space, and power constraints of the vehicle only with VHSIC 0.5 micron Phase 2 chips. Detailed design work has begun on customization of the Honeywell gate arrays and on increasing the yield (hence, the availability) of the chips. (Chapter 4, Section 4.2)

- A broadening of the industrial base for VHSIC capability has occurred as more and more manufacturers are providing 1.0 to 1.25 micron technology on certified production lines. The list of industrial suppliers of VHSIC shows a marked increase in the availability of products, design services, and foundry services for use by DoD contractors. (Chapter 3, Section 3.1)

- Since the adoption of the VHDL as the industrial standard for digital integrated circuit documentation (IEEE Standard 1076), an increasing number of new IC designs use the VHDL and the tool sets based on it. The Navy issued a data item description (DID OT-22047) to be used on contracts requiring VHDL descriptions (reference 1.11). During 1988, a consortium of industrial system designers, under the sponsorship of the Electronic Industries Association, began to develop a standardized format for VHDL chip models to be used within the VHDL design environment. Standardization of formats will accelerate the use of VHDL in board

design by providing greater compatibility between different sources of design data for standard parts. (Chapter 5, Section 5.1)

- An automated microcode computer synthesis and design system (AMSDS), under development by JRS Research Laboratories for the VHSIC program since 1984, has been successfully integrated with the VHDL (IEEE 1076 version). It has produced, analyzed, and simulated VHDL models of the Phase 1 VHSIC chips from Honeywell, Texas Instruments, and TRW. This unique design system has shown that the design of large, complex VHSIC class chips can, with proper software tools, be fast and efficient with little or no loss of code compactness compared to much more time consuming and error prone manual procedures. (Chapter 5, Section 5.1.3.2)

- As in past years, the VHSIC Program Office has sponsored a number of productive conferences and workshops during 1988 on VHSIC and VHSIC-related topics. These meetings are one of the best ways of providing the mechanism for easy and timely interchange of the information, data, and ideas which promote the rapid spread of VHSIC technology in consonance with the goals of the program (Appendix A, references 1.12 through 1.20, and Appendix B)

1.4 PROGRAM STATUS

The major activities during 1988 occurring under VHSIC Program Office sponsorship have been in the areas of 0.5 micron chip design and fabrication (Phase 2), system applications, pilot line certification and chip qualification (Phase 3), and in the collection of tasks related to design tools and software (Phase 3).

A few documentation and demonstration tasks remaining from Phase 1 are still being completed. Hughes Aircraft, for example, has scheduled a demonstration of its Phase 1 EPLRS brassboard in January 1989 using VHSIC-1 chips designed by Hughes and fabricated by AT&T. It is expected that final reports on Phase 1 will be received during 1989 from Hughes, Texas Instruments, and TRW.

The Phase 2 effort at IBM to develop a manufacturable 0.5 micron process has been successfully completed, the brassboard module has been demonstrated performing the ASW beamformer function, and all four of the Phase 2 submicron chips designed for this contract have been successfully fabricated at encouraging yield levels. Details are fully reported in Chapter 4. The 0.5 micron development efforts at Honeywell and TRW are still under way with the brassboard modules at each company scheduled for fabrication and demonstration in the second half of 1989.

As the VHSIC 1.25 micron technology has increasingly become the standard industrial level for advanced IC technology, the use of that technology as the basis for proposed new system developments has increased and the need for VHSIC funded system application projects

has decreased. This shift toward a full production line orientation for VHSIC products, as opposed to a pilot production operation, has thrown a burden on the DoD to accelerate the development of appropriate new qualification standards and procedures so that the acquisition of operational weapon systems with VHSIC products can proceed. The DoD has implemented the proposed changes in Requirement 64 of MIL-STD-454L reported in the VHSIC Annual Report for 1987. Requirement 64 governs the acquisition standards for microelectronic components and the higher performance standards included in the changes directly reflect the influence of VHSIC technology. DoD has also supported the development of generic chip qualification procedures based on qualifying the manufacturing lines which produce the chips and then controlling the quality and stability of the process line to ensure the integrity of the product. This method reduces substantially the burden of individual piece-part testing and has the potential for sharp reductions in cost.

The detailed status of the Phase 2, Phase 3, and Technology Insertion programs of the three Services is presented in the following sections of this report.

The technical reports issued thus far and other documents pertaining to the program are referenced in Appendix A. Appendix B lists the Conferences and Workshops sponsored by the VHSIC Program Office and some of the projected meetings scheduled for 1989. Appendices C and D provide points of contact within the DoD and industry for different parts of the program and identifying information on all of the current and past major contracts for the various phases of the VHSIC program. The glossary in Appendix E explains most of the acronyms used in this report.

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CHAPTER 2 - VHSIC TECHNOLOGY INSERTION

2.1 INTRODUCTION

"Technology Insertion" is the term used to describe the application of any of the products developed under the VHSIC program -- hardware, software, design tools, or standards -- to the acquisition of systems. Most of the prominent insertion projects in the past have been identified with the introduction of VHSIC chips (i.e. hardware) into operational weapon systems. However, VHSIC design automation technology can also be used in the development of a new system and in the maintenance or improvement of an existing one. It can contribute to improvements in the procedures and tools used to design, procure, or support military hardware. Thus, technology insertion constitutes one of the basic goals of the VHSIC program and a primary standard for its success.

Since hardware insertion necessarily involves the linking of "high tech" with operational military systems, it is also one of the more difficult problems that confronts the DoD. The systems used by the DoD go through a formal, complex acquisition process. It starts with a statement of the operational requirement which the system is to meet and ends with the deployment of the system in its operational mode. In between these two ultimate milestones are a large number of intermediate milestones and transition points -- system concept formulation and development, critical design reviews, technical demonstrations, initial engineering development, full scale engineering development, operational evaluation, production, training, logistics support. Each of these phases in the acquisition of the system must be planned and scheduled years in advance -- sometimes decades. The schedule and the budgets must be coordinated with and compete with many other defense requirements, with budget cycles, and often with national policies.

The manager of a system program has the serious responsibility of staying on schedule and within budget for the development of his system and yet have the system meet specified performance criteria and cost. Although the use of a new technology may offer the possibility of even better system performance or lower life cycle cost, the system manager may reasonably decide that the uncertainties associated with a new technology (e.g. with regard to assured sources of supply, long term reliability, and quality control) constitute unacceptable risks to his schedule and budget. Program managers must constantly balance the desire for "the best" against the need to meet planned deployment schedules, especially in the early stages of the system development.

The introduction of new design automation technology faces additional problems. Design data and procedures have traditionally been part of the commercial electronic world and have been highly proprietary. Therefore the adoption of VHSIC derived techniques and the development of VHSIC compatible tools for design automation depend heavily on the acceptance by the electronic industry of its need for particular tools and techniques.

The VHSIC program approach for meeting these challenges has been to support a substantial number of system hardware insertion projects and to actively encourage industrial

design groups to participate in the development of VHDL compatible design tools and the means for making the design data interchangeable among different users to the maximum extent.

The hardware projects described in Section 2.2 below are co-funded by the VHSIC Program Office and have been selected by the three Services to demonstrate that VHSIC works, that it is available, and that its use is beneficial. The benefits become manifest in different ways depending on the application -- increased performance, increased reliability, enhanced maintainability, reduced acquisition costs, less weight and space, or reduced life cycle costs.

Section 2.3 lists the independent insertion programs in the systems applications area. They are not directly funded by the VHSIC Program Office but they use the advanced VHSIC microelectronic hardware in system developments. Section 2.4 lists a number of industrial companies that are developing design tools which will work in the VHDL environment and interface that environment to many of the commercial design tools that already exist. Some of these programs began with VHSIC seed money and are continuing as commercial projects. Collectively, these VHSIC technology insertion efforts reflect the growing activity by DoD contractors and by the commercial electronics industry in introducing VHSIC products and technology into military systems.

For each of these technology insertion projects, Appendix D lists a point of contact in both the sponsoring Service and the contractor.

2.2 VHSIC SYSTEM INSERTION PROJECTS (VHSIC PROGRAM FUNDED)

2.2.1 ARMY

2.2.1.1 Enhanced PLRS User Unit (EPUU)

The PLRS (Position Location and Reporting System) is designed to provide Army ground troops with a system for battlefield tactical data transmission. A VHSIC version of the EPUU which will have a three-fold increase in signal throughput is being developed by Hughes Aircraft for the Army CECOM. The increased capacity is needed to meet the growth anticipated in the volume of data which must be electronically exchanged on the battlefield. A VHSIC chip set that will update the Signal Message Processor (SMP) module in the EPUU has been designed by Hughes Aircraft and fabricated by AT&T. There are also plans to design a second chip set for a second module in the EPUU. These two VHSIC modules will also reduce both the logistics and acquisition costs associated with the planned production of more than 20,000 EPUUs. Preliminary Government estimates indicate that over $100 million can be saved in acquisition and life cycle cost by this use of VHSIC components in the PLRS system.

On December 11, 1986, Hughes demonstrated the fully functional VHSIC-1 devices which transferred messages between a brassboard VHSIC EPUU and standard units. See references 2.1 and 2.2. On March 3, 1988, the contractor demonstrated that the EPUU brassboard had a threefold increase in signal throughput over current designs. Preliminary results indicate that the performance of this EPUU is better than predicted by mathematical models.

The EPUU brassboard contract will be completed by March 1989 with acceptance demonstrations and delivery of the brassboard hardware.

During the last quarter of 1988, a single chip four-section correlator was fabricated by AT&T to replace the four separate single-section correlator chips now used. This new chip is to be used in the prototype SMP modules which are scheduled for testing in May 1989. The modules will be integrated into twelve prototype VHSIC EPUUs which will be demonstrated and then undergo performance testing during 1989. See Figure 2.1.

2.2.1.2 Light Helicopter Program (LHX) Mission Computer

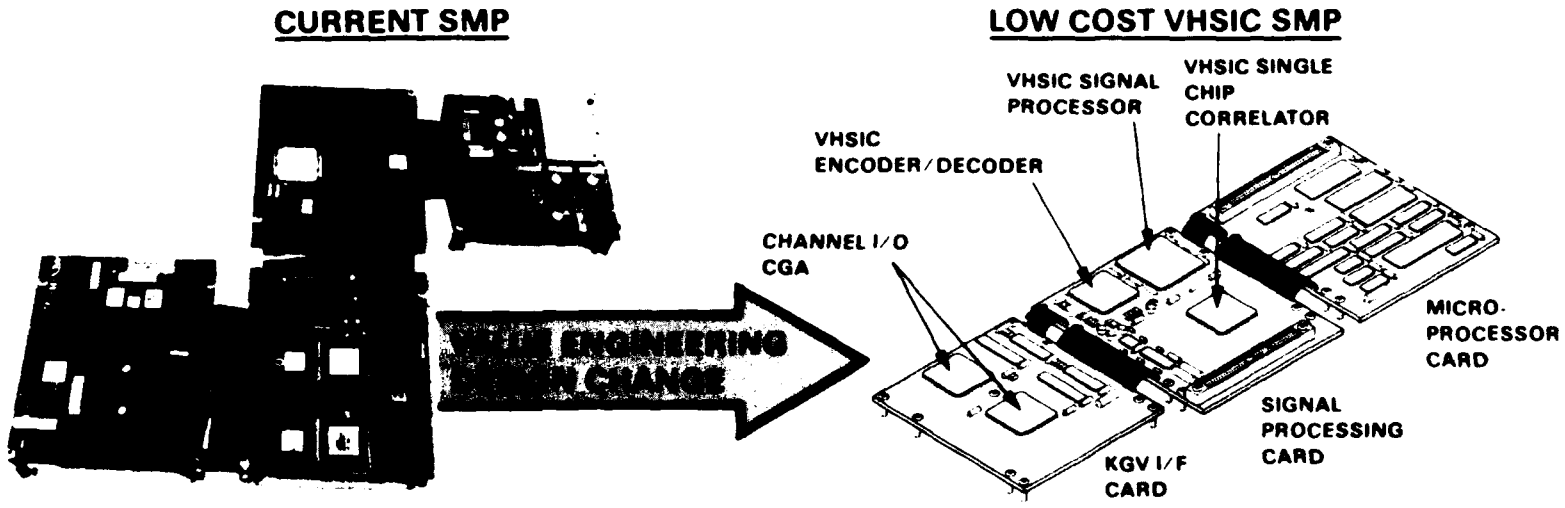
During 1985 and 1986, design work on advanced cockpit and mission equipment for the LHX helicopter program included a task to provide preliminary designs of a mission computer using VHSIC chips. This design effort was jointly funded by the Army AVSCOM LHX Program Office and the VHSIC Program Office. See references 2.3 through 2.7.

The LHX contractors have since formed into two teams - Boeing/Sikorsky and McDonnell/Bell. Using the preliminary mission computer designs as a base, each of the two LHX contractor teams has continued the design of a VHSIC version of the computer during 1987/1988. The contractor teams have demonstrated selected features and functions of breadboard signal and data processors, memory management, sensor data distribution, video processors, and bus interface modules. The design of the LHX depends on a high degree of automation in the helicopter platform and mission systems. With the weight and space limitations of the platform, the mission requirements can best be met with a VHSIC computer. Using alternative, less capable technologies, will result in a more limited system performance. The specific chips to be designed and the fabricator of these chips are to be determined.

These detailed mission computer design efforts have reduced the technical risk to acceptable levels for the beginning of the formal DEM/VAL program. The DEM/VAL effort began in November 1988 and will run for 23 months. Upon completion of this effort the government will select one contractor team to continue into the formal FSD program to begin in December 1990. Development and formal laboratory demonstration of a complete VHSIC mission computer capability (to include all module types) is part of the DEM/VAL program.

VHSIC INSERTION INTO THE EPLRS SIGNAL AND MESSAGE PROCESSOR

HUGHES



	CURRENT SMP	VHSIC SMP
• NUMBER OF CIRCUIT CARDS	4	3
• ESTIMATED PRODUCTION COST	$4,997	$4,429
• NUMBER OF DEVICES	72 VLSI, 1 HYBRID	23 VLSI DEVICES, 3 VHSIC DEVICES
• PREDICTED RELIABILITY	30,000 HRS MTBF	43,500 HRS MTBF

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Figure 2.1 - Hughes Insertion Into EPLRS

2.2.1.3 TOW Missile Automatic Target Tracker

The goal of the TOW (Tube-launched, Optically-tracked, Wire-guided) missile insertion program is to demonstrate a VHSIC brassboard which can track two targets simultaneously and provide guidance signals to the missile. The TOW system will benefit by having greater accuracy and an increased rate of fire with simplified training requirements for the operator. The new, automatic, multiple target tracking capability could not be provided within the weight, power, and volume constraints of the present system without VHSIC technology.

The brassboard development was awarded to Texas Instruments in 1985 by the Army MICOM. System design and some chip fabrication and software development were completed by the end of 1986. At the beginning of 1987, TI completed the system design, chip fabrication, and hardware assembly and software integration and test were well underway.

During 1988, program management was shifted to DARPA via a new contract. The system assembly was completed, laboratory tested, and installed in a field test van. Static target tracking tests were begun in December.

After successful demonstration, the automatic target tracker technology will be available for use in the TOW, the Advanced Anti-Tank Weapon System, and the tri-Service Hyper-Velocity Missile projects. See reference 2.8.

2.2.1.4 Firefinder Radars

The Army LABCOM (Electronics Technology and Devices Laboratory) is developing a high performance VHSIC signal processor for the Firefinder radar systems. The processor will permit a significant reduction in size and improvement in performance and survivability of the Firefinder radar systems.

The Firefinder radars detect sources of hostile mortar, artillery, and rocket fire and accurately compute their location for the direction of counterfire. The use of VHSIC technology in the signal processor will significantly improve the performance of the weapon location computation, provide classification of the weapon type, and enhance the system performance against EW threats. The VHSIC processor reduces the power by 60% and the parts count by 75%, which makes it a key subsystem in evolving toward a single vehicle Firefinder system. Installation of the radar on a single vehicle will reduce the crew size from eight to four personnel for the AN/TPQ-36 version of the radar. The total projected life cycle cost savings is $430 million.

At the beginning of 1988, a single processor module was assembled using four VHSIC chip types that had been designed by Hughes Aircraft and fabricated by LSI Logic. Application software for operation of the processor in the radar system was being developed.

During 1988, the number of processor modules being assembled for the program was increased to eight so that the radar data could be processed in a real time. The eight VHSIC modules, along with ten other non-VHSIC modules, were integrated by Hughes into a demonstration brassboard. Application software for the processing of radar signals was written and debugged. The brassboard processor was integrated into an existing Firefinder radar, and a demonstration of advanced electronic survivability for radar systems will be performed in January 1989. See reference 2.9.

2.2.1.5 Common Module VHSIC Integrated System (CVIS)

The Army Armament Research Development and Engineering Center (ARDEC) is developing a standard signal processing system that is applicable to the M1 tank and other ground combat vehicles and air combat vehicles, such as helicopters. The program, now called the Common Module VHSIC Integrated System (CVIS), formerly called Combat Vehicle VHSIC Integrated System, will produce a design that includes a family of functional circuit modules, a package design for the modules that meets ground combat vehicle operating requirements, a software operating system that supports applications written in Ada, and a field programming unit that supports software debugging on the hardware.

The CVIS family of modules includes a 1750A data processor, array processor, global memory, 1553B interface, and several other I/O modules. The modules interface to the VHSIC Phase 2 Pi-Bus and will be packaged on double-sided surface mount SEM-E circuit modules. Increased speed, as well as reductions in weight, size, and power are expected through the use of VHSIC chips. The contractors are General Dynamics and Westinghouse. Westinghouse chips will be fabricated by National Semiconductor Corporation.

2.2.1.6 Miniaturized Electronic Direction Finder Location Indicator (MEDFLI)

The goal of the Army CECOM MEDFLI program is to produce small, lightweight EW payloads for airborne and ground applications that can handle the severe threat emitter environment of the 1990s and beyond. The contractors for this program are ESL Corporation and General Electric. The chips being used are a General Electric reduced instruction set compiler (RISC) and Raytheon FIFO and gate array chips. The goal of this insertion project is to improve the throughput and reliability of the MEDFLI signal processor and to develop a special purpose Threat Association Module (TAM) for unique EW processing applications.

Fabrication of the TAM began early in 1986. During 1987, the TAM Module was completed and successfully demonstrated, and a contract for fabrication of the VHSIC Modular Adaptive Signal Sorter (VMASS) was awarded in August 1987, with

completion expected in late FY89. See references 2.10 and 2.11.

The VMASS processor is the digital EW signal processor tentatively slated to be used in the next generation MEDFLI Unattended Airborne Vehicle (UAV) ELINT/ESM payload, known as "Silent Fox".

The VTAM and VMASS processors will be integrated in FY89 and FY90 for a full system demonstration.

2.2.1.7 Hellfire Imaging Infrared Seeker

The Imaging Infrared (IIR) seeker for the Hellfire Fire and Forget missile system requires a signal processor with high data throughput, but which is very small, light weight, and low powered. Only through the use of VHSIC technology in the seeker and processor can this be accomplished. The objective is a more reliable, lower cost seeker with a long shelf life and built-in-test capability. The programmable/modular nature of the VHSIC components will also accommodate future upgrades of missile capability.

Development contracts for a VHSIC processor for the seeker were awarded by MICOM in September 1985 to Texas Instruments, McDonnell-Douglas, and Ford Aeronutronics. At the beginning of 1987, development of the VHSIC processor hardware for insertion into the Hellfire IIR seeker was well under way. However, the Joint Services Seeker program, which was to furnish the sensor hardware for insertion into the Hellfire system, had been terminated. See references 2.12-2.14.

In order to complete the program, the Texas Instruments Hellfire VHSIC insertion contract was modified to include the fabrication of a seeker head. The other contractors continued work only on the processor electronics.

During 1988, the TI and McDonnell efforts were discontinued, but the Ford program produced a promising processor development based on a gate array designed by Ford Aeronutronics and fabricated by Ford/LSI. The resulting processor will be delivered to MICOM during 1989 for in-house experimentation.

2.2.1.8 Multi-Role Survivable Radar (MRSR)

The Multi-Role Survivable Radar is being designed by the Army MICOM to make the operation of air defense artillery more effective in a combat environment that includes anti-radiation missiles and electronic countermeasures. The MRSR minimizes the ARM and ECM threats by using frequency agility over its operational bandwidth and by using a very low peak power level.

A prototype of the MRSR is now being assembled by Raytheon using chips of its own design and fabrication. This technology insertion study, started in January 1987, is nearing completion. A VHSIC processor for the MRSR appears to be achievable by the time the MRSR is ready for delivery in late 1990 or early 1991.

2.2.1.9 Army Command and Control System (ACCS)

The objective of this Army CECOM study is to determine whether the interoperability between ACCS and supporting systems can be improved by using VHSIC products.

The study started in February 1988 and the final report is expected in February 1989. The first six months were devoted to studying the different ACCS interfaces and assessing the feasibility of using VHSIC technology. An interim report was completed in July 1988. The last part of the effort is being devoted to a detailed study of a specific area of interest within the ACCS interfaces. No hardware is being produced. See reference 2.15.

2.2.2 NAVY

2.2.2.1 MK-50 Advanced Lightweight Torpedo (ALWT)

The MK-50 ALWT is being developed by Honeywell for the Naval Sea Systems Command as the next generation torpedo for use against the continually evolving Soviet submarine threat. It will be the primary ASW weapon for air and surface platforms as well as the principal submarine standoff weapon.

VHSIC insertion provides significant benefits to the MK-50 system: a saving of 5 inches in length and 40 pounds in weight which could be allocated to a larger warhead; increased reliability by having 1,300 fewer components and 15,000 fewer solder joints; power reduction of 16 watts; and 540 square inches less circuit board area. The overall result is a reduction in acquisition cost of approximately $10,000 per torpedo, as well as a reduction in life cycle costs because of better reliability and maintenance characteristics with the same or better performance parameters. By adding the increased capability of a single board AN/AYK-14 computer (which is a separate VHSIC insertion program described below) the size and weight of the electronics section of the torpedo would be reduced even more.

VHSIC Phase 1 chips from several different manufacturers are being used in the digital receiver and in the command and control subsections. These include the TRW micro-controller chip, the TRW address generator chip, the TI SRAM, and a number of ETA/Honeywell gate array personalizations.

During 1988, environmental testing of the memory board for the command and control subsection was completed and this module is ready for insertion into the torpedo during the first full production contract. Work will begin on the VHSIC signal processor for this subsection in 1989. The digital receiver breadboard failed to operate

at the required speed because the interconnect design of the circuit board was inadequate; therefore a redesign is required. Work will continue on the digital receiver as part of the MK-50 P^3I program.

2.2.2.2 HF/EHF Communications: VHSIC Terminal Brassboard (VTB)

The VHSIC Terminal Brassboard (VTB) is part of a joint Navy/Air Force project to assess the ability of VHSIC technology to meet the requirements for new, complex processing of communications signals. The VTB is designed with a common architecture for processing the signal waveforms received from both the High Frequency Anti-Jam (HFAJ) system and the Milstar EHF satellite system. The VHSIC terminal design is projected to reduce the size, weight, and power by 75% from current terminal designs. Significant improvements in reliability, maintainability, and long term system costs are also expected. These benefits will make it possible to receive EHF, HFAJ, and other sophisticated communications signals on submarine and manpack terminals where very limited space and power are available.

The VTB is being developed by TRW for the Space and Warfare Systems Command. The design and fabrication of the chips for the VTB were completed during 1987, making extensive use of TRW chips developed during Phase 1 and under the VCP insertion program discussed below in Section 2.2.2.4. The chips include a flexible VHSIC signal processor, an FFT chip set, a convolutional decoder, and a configurable gate array.

Development, fabrication, and integration of the VTB is nearing completion. Extensive testing of the EHF portion of the system will be conducted at the Milstar test bed located in San Diego at the Naval Ocean Systems Center (NOSC) during the first quarter of 1989. Preliminary testing will use a satellite simulator at NOSC. On-the-air testing with the FLTSAT EHF Package (FEP) satellite (a precursor to Milstar), is also being considered. HFAJ testing details are still being defined based on changes in the Navy's program development efforts in this area. It is anticipated that the VTB test data and architecture concepts will be major factors in the design of emerging submarine and special forces radio systems.

2.2.2.3 AN/AYK-14(V) Standard Airborne Computer

The AN/AYK-14 Navy Standard Airborne Computer is a modular, general purpose digital computer that is used in most naval aircraft. This computer is functionally and physically partitioned into replaceable modules to provide operational flexibility. The computer is used in such platforms as the E-2C, EA-6B, P-3C, F-14D, A-6, EP-3, AV-8B, F/A-18D, SH-60B, A-12, MK-50, and the Automatic Carrier Landing System. Production quantities of 12,000 to 14,000 units are expected by 1995.

Control Data Corporation was awarded a contract by NAVAIR in February

1986 to develop a VHSIC version of this computer. The VHSIC Processor Module (VPM) will provide a five fold improvement in performance, store one million words of local memory on the module, be interchangeable with previous processor modules, and have an MTBF in excess of 10,000 hours.

The five VHSIC chips for this development are based on 1.25 micron technology and are currently being fabricated by VTC, Inc. using standard cell designs and by LSI Logic using customized gate arrays. It is expected that chip fabrication will be completed in early 1989 and that a laboratory version of a VPM module will be demonstrated by mid-year. Deliveries to F-14, F-18, and EA-6B aircraft in 1990 and beyond are expected to require the production of three to five thousand systems using a correspondingly larger number of chips.

Several test chips have been fabricated during 1988. The purpose of these chips was to confirm performance and functionality of several custom macrocells, a sophisticated on-chip maintenance system, and correlation of simulation results to silicon results. All of these test chips have been analyzed with successful results.

2.2.2.4 VHSIC Communications Processor (VCP)

The objective of this program is to demonstrate the improved performance of a communications processor which uses VHSIC technology. The VCP consists of a core signal processor in SEM-C format, and a preprocessor that provides matched filtering. The processor architecture was developed by TRW during VHSIC Phase 1 for an EW brassboard. Derivatives of the VCP are being used in the ICNIA program and the VTB program described above in Section 2.2.2.2. Each of the modules makes use of TRW VHSIC-1 chips.

In the VCP, the preprocessor will digitize baseband analog waveforms from an RF front end and pass them to the signal processor for digital demodulation and filtering. The VCP program successfully demonstrated the demodulation of GPS, Link 11, and AM voice signals in December 1988. Concurrent processing of multiple signals will be performed.

During 1988, two terminals using the VCP were assembled, and integration and testing was started. Acceptance test and delivery of the units are expected in early 1989.

2.2.2.5 AN/SRS-1 Combat Direction Finder

This program is the result of a Sanders Associates IRAD study which demonstrated the greatly improved processing throughput of a vector product calculator (VPC) using VHSIC components. The technology insertion effort was initiated by SPAWAR in November 1985 with the goal of production in 1988.

In February 1987, the initial phase was completed (thirteen months after the

start of the contract) with the design, development, and demonstration of a brassboard model of the VPC. It showed that the selected Phase 1 VHSIC chips from IBM, TRW, TI, and Motorola can be integrated with conventional logic components to achieve the design goals. The VPC was also designed to be used as an FFT engine in addition to its initial role as a generic array processor.

The second phase of this program, begun in March 1987, was to use gate arrays for the non-VHSIC chips in the VPC in order to reduce the number of circuit cards from four to one. This was accomplished and the VPC was successfully tested in the fourth quarter of 1988.

The VPC is scheduled to be integrated into the appropriate AN/SRS-1 subsystems and field tested in the summer of 1989. Production will follow formal system level operational test and evaluation.

2.2.3 AIR FORCE

2.2.3.1 Advanced Onboard Signal Processor

The purpose of the Advanced Onboard Signal Processor (AOSP) program at RADC is to develop spaceborne distributed processors that can provide the real-time signal processing capabilities required for future operations. The emphasis in this program has been on the development of a radiation hardenable vector processor (RHVP) that can function as an application processor unit (APU) within an AOSP architecture. VHSIC technology is being utilized to improve the hardware reliability, increase the processing capacity, and reduce the size, weight, and power consumption.

Contracts were awarded to IBM and TRW in September 1986 for the development of RHVP hardware. IBM has designed a high performance, Ada programmable, vector processor brassboard and has independently developed a radiation hard fabrication process. The chip designs are nearing completion and chip fabrication is scheduled to begin in January 1989. The brassboard hardware is scheduled to be completed in November 1989. The vector processor is being designed to work as a co-processor with the Generic VHSIC Spaceborne Computer (GVSC) in a manner that allows concurrent vector and scalar processing. The Boost Surveillance and Tracking System (BSTS) program office has expressed an interest in utilizing the RHVP in their ground demonstrations.

The TRW program has been changed to a study effort to design a processor which meets BSTS onboard processing requirements. The chip designs will be documented and completed in January 1989.

2.2.3.2 Cruise Missile Advanced Guidance (CMAG) Program

The objective of the Cruise Missile Advanced Guidance (CMAG) program of the Wright Aeronautical Laboratories is to design, fabricate, and test advanced guidance approaches applicable to future cruise missiles. The primary approach being taken is the use of compact laser radar sensors with high speed digital processors and advanced algorithms.

The CMAG VHSIC insertion program at Honeywell will develop and fabricate the chips for an alternative processor for the Advanced Guidance Unit (AGU) which is an existing system development program at General Dynamics. The goal of the program is to demonstrate submicron VHSIC technology performing critical processing functions within the cruise missile AGU test-bed. The submicron gate arrays now under development by Honeywell as part of the VHSIC Phase 2 submicron program will be used. The chips will be designed to work in the laser radar image processing modules to be inserted into the VHSIC Integrated Processor (VIP) developed by General Dynamics under IRAD. Supplemental chip design at Honeywell and the work at General Dynamics began in September 1988.

2.2.3.3 Common Signal Processor (CSP)

IBM has developed a modular common signal processor (CSP) for AFWAL based on VHSIC technology. It can be configured and programmed to process signals in a wide variety of applications such as high performance radars, secure communications, electronic warfare, image processing, and anti-submarine warfare. This program demonstrates the feasibility of a common signal processor which makes use of VHSIC technology to increase system performance without increasing weight, space, and power. Issues such as functional partitioning, module definition, standardization levels, and signal processor software development are being examined.

The ten 1.0 micron CMOS VHSIC chips that were developed under this effort during 1987 and 1988 have been used to design six CSP module types. These modules, in turn, have been used to build the CSP brassboards which were delivered in June 1988. The brassboards have been provided to Westinghouse for use on the Ultra-Reliable Radar program. Westinghouse is now integrating the CSP units with the Texas Instruments solid state phased array (SSPA) antenna and their own receiver subsystem. IBM continues to support Westinghouse in this effort. See Figure 2.2.

2.2.3.4 VHSIC Avionics Modular Processor (VAMP)

Westinghouse Electric Corporation (WEC) has designed and fabricated a breadboard model of the VAMP processor for AFWAL using VHSIC chips. The chips

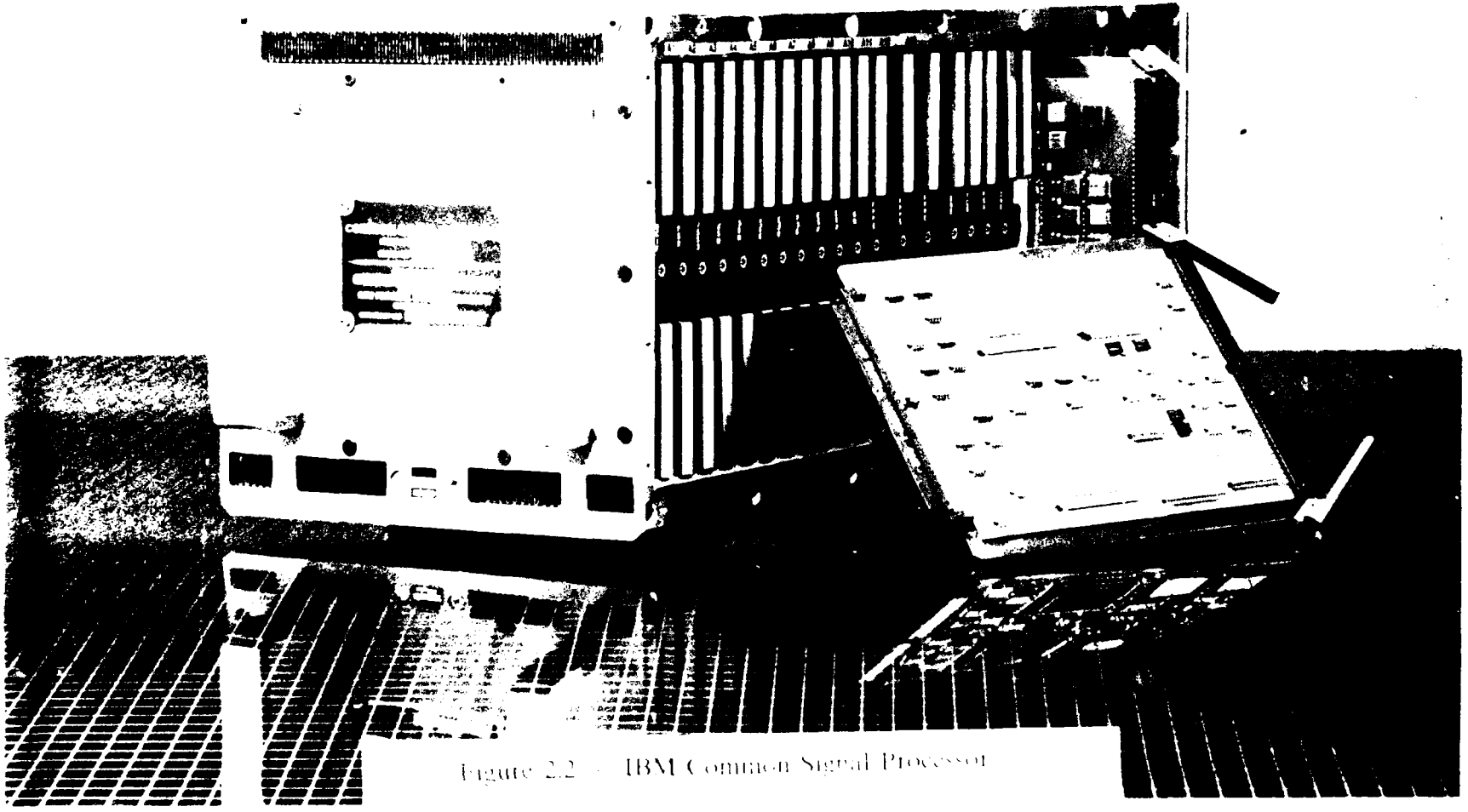


Figure 2.2 — IBM Common Signal Processor

were designed by Westinghouse and fabricated by the National Semiconductor Corp. The VAMP processor includes the 1750A processor function in addition to other processing functions. WEC is now in the process of fabricating six Advanced Development Models (ADMs) for delivery beginning January 1989. Two additional ADMs are being manufactured to fulfill a bilateral agreement with France.

2.2.3.5 Speech Enhancement Unit (SEU)

The Speech Enhancement Unit (SEU) is a speech processor that removes tone, impulse, and wideband noise from speech channels. The work is being done by Martin-Marietta for RADC. The SEU greatly improves the intelligibility of voice communications for both human operators and speech recognition equipment. VHSIC technology is required to make SEUs in a practical size for field deployment and at an affordable price. The chips used in the SEU were designed and fabricated for Martin-Marietta by AT&T. The increased throughput and speed of VHSIC devices will also provide better performance.

The SEU utilizes high speed commercial microprocessors and memories and VHSIC gate arrays. The gate array designs and the brassboard design are in progress. Two boards will be completed in FY89, and the project is scheduled to be completed in September 1990.

2.2.3.6 Milstar Terminal/Modem Processor

Milstar is an EHF satellite communication system. The use of VHSIC technology will provide improved performance with reduced weight, space, power, and life cycle cost. It will become possible to install the Milstar terminal on platforms with space and weight restrictions that otherwise preclude such installation.

The program started at TRW in 1984. The processor uses the preprocessor portions of the EHF on-board brassboard plus additional Phase 1 convolutional, fast Fourier transform, and multiplier/accumulator chips designed and fabricated at TRW. For the related Navy effort on the VHSIC Terminal Brassboard (VTB), see Section 2.2.2.2 above.

2.2.3.7 F-15 Central Computer

The F-15 central computer controls pilot displays, weapon launch systems, and the aircraft g-load warning system. An IBM VHSIC 1750A computer forms the basis for this program. IBM is a subcontractor of McDonnell Douglas in this effort for the Air Force.

The program began in June 1988. The hardware preliminary design review (PDR) is scheduled for March 1989. The software PDR is scheduled for June 1989.

Installation into F-15E fighters is scheduled for April 1992.

2.2.3.8 AN/APG-68 Radar VHSIC Programmable Signal Processor (VPSP)

The AN/APG-68 is an airborne fire control radar on the F-16 aircraft, which is being developed by Westinghouse for the Air Force, to provide air-to-air target detection and tracking. A VPSP will greatly improve the operational characteristics of the radar such as tracking range, target discrimination, and multiple target tracking. The program began in 1985 and the first phase was completed with a successful brassboard demonstration.

2.2.3.9 E-3A Signal Processor

The E-3A Sentry aircraft is the Air Force Airborne Warning and Control System (AWACS). This insertion effort by the Air Force is aimed at improving the performance and logistics characteristics of the signal processor used in the surveillance radar on board the Sentry.

Westinghouse completed an initial system insertion study in 1983. The follow-on design phase was completed in 1985 and a contract award for the hardware phase was made in August 1986. A systolic vector processor based on the Westinghouse RPLAU chip was demonstrated in 1988. Full scale development is expected to begin in April 1989.

2.2.3.10 Air Logistics Center - Sacramento

Numerous Air Force electronic systems contain older transistor-transistor-logic (TTL) devices which are rapidly becoming unavailable. The result is a generation of front line weapon systems that may soon become very difficult and expensive to maintain in operation. Many of the older components are also relatively unreliable which makes the system "go down" frequently, thus compounding poor maintenance with poor availability.

For both of these reasons the Air Logistics Center at Sacramento (SM-ALC) has undertaken a number of VHSIC insertion projects with partial funding from the VHSIC Program Office. The approach taken by the SM-ALC has been to use in-house facilities to customize commercially produced VHSIC gate arrays which can then perform the function needed to replace specific chips. If necessary, the customized gate array can be packaged to provide a "form, fit, and function" replacement for an obsolete or unreliable part.

One of the first projects undertaken by SM-ALC was the design, fabrication, and testing of a VHSIC replacement for the Signal Interface Board in the F-111D Digital Signal Transfer Unit (DSTU). This was completed in August 1987 using gate

arrays fabricated by Rockwell and personalized by SM-ALC. Two replacement boards were inserted into two operational aircraft at Cannon AFB and, as reported in the VHSIC 1987 Annual Report, became the first operational use of VHSIC. Since the installation, the units have accumulated more than 2000 hours of flying time. The new board has increased MTBF from 40 hours to a projected 5000 hours, costs $3500 versus $24,000, has built-in test and fault isolation, and provides a form, fit, function replacement for the previous board. Fifteen production boards will be delivered in April 1989 for installation in flight-line aircraft. A second source for the gate arrays is being developed at National Semiconductor.

To expand this activity to include replacement of more parts, SM-ALC has written specifications for a generic gate array which can emulate over 300 TTL parts by customization. SM-ALC plans to provide the customization data to the contractor, Honeywell, for final fabrication after which the chips will be tested at SM-ALC. Honeywell delivered 5 prototype gate arrays in October 1988 and is scheduled to deliver 11 more during the last half of 1989.

Using this approach, SM-ALC plans to design a VHSIC based modular 1750A microprocessor with extensive BIT/FIT and integrated diagnostics. These modules will then be used to upgrade the reliability of the communication multiplexer in the Cheyenne Mountain complex from 60 hours MTBF to 5000 hours. At the same time it is projected that the mean-time-to-repair will decrease from 2 weeks to 10 minutes, the spares count will be reduced by 90%, and eight racks of equipment will be replaced by one. Some of the same modules will also be used in an upgrade of the AN/FPS-117 air surveillance radar at Cheyenne Mountain. For this insertion, the projections are an MTBF increase from 700 to 5000 hours, prime power reduction from 17 KW to 1 KW, reduction from 5 racks to 1, and the capability to use advanced software for improved radar performance.

2.3 VHSIC SYSTEM INSERTION PROJECTS (OTHER FUNDING)

This section lists VHSIC insertion projects which are supported by funding other than from the VHSIC program. The list includes projects sponsored by various Service system program (and other) offices and by IRAD and other industrial funding. Figures 2.3 and 2.4 below illustrate applications of some these projects.

2.3.1 General Dynamics

- o Cruise Missile Advanced Guidance (AF)
  - 0.5 micron bipolar (Honeywell)
  - PI bus and TM bus interfaces

- o Avionics 1750A microprocessor (AF)
  - 1.25 micron CMOS (NSC)
  - one chip design
- o M1A2 Tank serial data bus controller (Army)
  - 1.0 micron CMOS (VTC)
  - prototypes demonstrated

Contact: P. Hedtke (619) 547-3787 (CMAG)
General Dynamics - Convair
Kearny Mesa Facility (MZ-41-6590)
P.O. Box 85357
San Diego, CA 92138

J. Marcks (817) 763-4491 (1750A)
General Dynamics
P.O. Box 748
Fort Worth, TX 76101

C. Schauss (313) 362-8193 (M1A2)
General Dynamics Land Systems
1902 Northwood
Troy, MI 48084

2.3.2 General Electric - 1.25 micron CMOS, bulk and SOS

- o SABIR (SDIO) - 13 prototype chips
- o SADARM 13-bit microprocessor (Army) - designed with silicon compiler
- o Remote Battlefield Surveillance System (Army) - chips in prototype stage
- o Aegis 1750A (Navy) - single chip, prototype

Contact: J. Emory Lane (919) 549-3100
GE Microelectronics Center
P.O. Box 13049
Research Triangle Park, NC 27709-3049

2.3.3 Honeywell - CMOS 1.25 micron, bipolar 1.25 micron

- o Military computer module (Army) - chips for prototype delivered
- o Enhanced modular signal processor (AT&T) - test modules delivered; first prototype module in 06/89
- o Generic VHSIC spaceborne computer (AF) - breadboard demo completed

Generic VHSIC Spaceborne Computer (GVSC)

VHSIC SUBMICRON

Honeywell

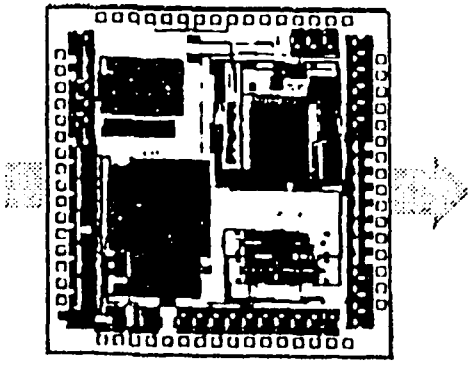
Customer: USAFSTC

Purpose: To develop a radiation-hardened, high-performance 1750A chip set

Status: Contract 1985-1989
Phase 2 underway

Honeywell Role

- To design, develop, and produce a radiation-hardened, high-performance 1750A chip set
  - >3.0 MIPS
  - RICMOS technology
  - >SDI levels
- To assist in the application of these chip sets in defined opportunities
- To characterize these chips both functionally and environmentally



Results

- All five chips functional
- GVSC wirewrap breadboard operating at 20-MHz

⇒ DAIS mix performance 3 MIPS

- GVSC microwire brassboard will improve performance
- 64K x 1 RAMs in package

Figure 2.3 - Honeywell Generic VHSIC Spaceborne Computer

- o Boost surveillance tracking system (AF) - demo of processor in 05/90
- o Milstar (AF) - chips in production
- o Trident (Navy)
- o DSP (DoD)
- o Mars Observer (NASA)
- o Radiation hard 32 bit processor (AF) - system eval chips in design
- o ATF display processor (AF)

Contact: G. Anderson (612) 541-2015
Honeywell SSED
12001 State Highway 55
Plymouth, MN 55441

2.3.4 Hughes - CMOS/SOS 1.25 micron, CMOS 1.1 micron

- o Airborne dipping sonar (Navy)
- o Timing bus monitor (Army)
- o Multi-Mission Bus spacecraft (Various)
- o AUSSAT (Australian communications satellite)
- o UHF follow-on to LANDSAT (Navy)
- o Hughes satellite HS-601 (Various)
- o LHX Vista (Army)
- o D3 fire control system (Army)
- o ATF VSP network with PI-BUS, TM-BUS, VHDL (AF)
- o Light weight exoatmospheric projectile (SDIO)
- o Mark 48 ADCAP torpedo (Navy)

Contact: R. Dodge (619) 931-3196
Hughes Microelectronics Center
6155 El Camino Real
Carlsbad, CA 92009

2.3.5 IBM - CMOS 1.0 micron and 0.5 micron

- o Radiation hard 32-bit processor - RH32 (AF)
- o Boost surveillance tracking system (AF)
- o TACJAM phase II (Army)

Contact: W. T. Cahill (703) 367-3925
IBM Federal Systems Division

9500 Godwin Drive
Manassas, VA 22110

2.3.6 Raytheon - CMOS 1.25 micron

- o Tartar missile (Navy)
- o Advanced processor for air-to-air missiles (AF)
- o Advanced on-board signal processor (AF/DARPA)
- o Ground based radar (Army)
- o Milstar (AF)
- o AMRAAM missile producibility enhancement (Navy/AF)
- o IR Maverick AGM-65D (AF)
- o AIM-54C Phoenix missile (Navy)
- o Aegis standard missile (Navy)
- o Sparrow missile (Navy)
- o AN/SLQ-32 (Navy)
- o Mk-XV IFF (AF)

Contact: F. X. Wright (617) 860-2251
Raytheon
141 Spring Street
Lexington, MA 02173

2.3.7 Texas Instruments - CMOS 1.25 micron

- o ATF YF-22 mission display processor (AF) - flight demonstration in 1989
- o M1A1 tank automatic target tracker (Army) - demonstrated in 1987; continuing under CVIS at General Dynamics

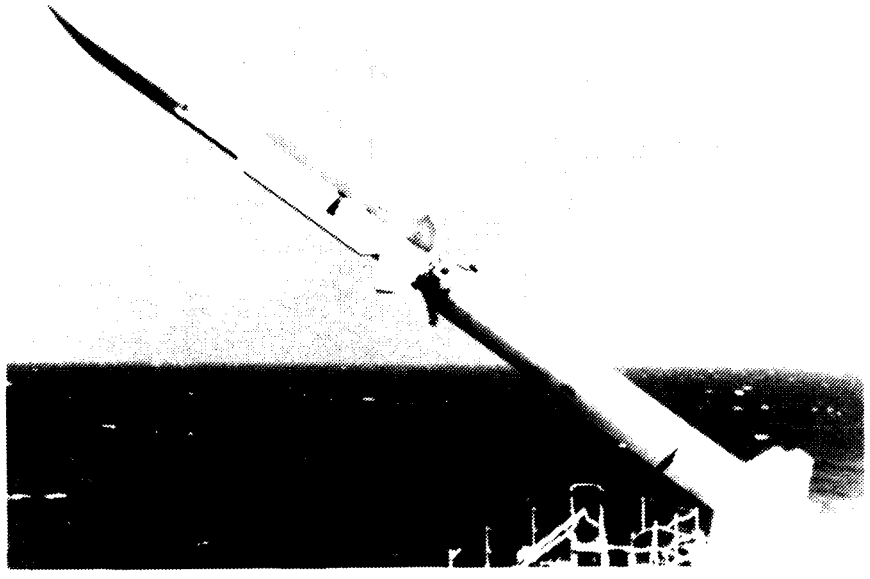
Contact: J. Coumelis (214) 575-3530
Texas Instruments
P.O. Box 869305, MS8435
Plano, TX 75086

2.3.8 TRW - CMOS 1.25 and 0.5 micron

- o Radiation hard 32-bit computer (AF) - in development
- o Radiation hard vector processor (AF) - in development
- o ICNIA (AF)

Standard Missile-2 Block IV AEGIS ER

- VHSIC Insertion
  - — Digital Signal Processor
- VHSIC Chips
  - — FFT
  - — Control
  - — I/O
- 3:1 Parts Reduction with 8:1 Throughput Improvement
- Projected Production Quantity of 6000 Units



TERRIER

NAVY
NAVAL SEA SYSTEMS COMMAND
(NAVSEA)

Figure 2.4 - Raytheon Insertion Into Aegis

- o INEWS (AF)
- o Battle management processor (Army) - 0.5 micron study
- o Cryogenic CMOS for focal plane array (Navy) - in development
- o Mass memory subsystem (AF) - in development
- o Advanced spacecraft computer module (AF) - study
- o Aladdin submunitions processor (DARPA) - 0.5 micron study
- o SEP Standard EHF Package (AF) - in development
- o Advanced communications signal processor (Navy) - 0.5 micron
- o ATF digital avionics (AF) - 0.5 micron CPUAX study

Contact: T. A. Zimmerman (213) 814-2400
TRW Electronic Systems Group
One Space Park
Redondo Beach, CA 90278

2.3.9 Unisys - CMOS 1.25 micron

- o ATF 1750A (IRAD) - prototype
- o AN/UYK-44 (IRAD) - prototypes
- o Radiation hard 32-bit processor (AF) - simulate in 1989

Contact: J. F Stewart (612) 456-3858
Unisys Defense Systems
P.O. Box 64525
St. Paul, MN 55164-0525

2.3.10 Westinghouse - CMOS 1.25 micron

- o Joint Stars radar processing subsystem (AF) - study
- o Common module integrated system (Army) - demonstrate in 1989
- o High speed programmable signal processor (IRAD) - prototype
- o General purpose avionics data processor (AF) - demonstrated in 1988

Contact: D. Sartorio (301) 765-6744
Westinghouse
VHSIC and Digital Systems Dept.
719 Hammonds Ferry Road
M.S. 5210
Linthicum, MD 21090

2.4 COMMERCIALLY AVAILABLE VHSIC DESIGN TOOLS

The following list is a sample of the companies that are developing design tools which directly support the VHDL in various software tools areas.

Simulators/Analyzers

2.4.1 Intermetrics

Description: VHDL analyzer and simulator targeted to UNIX and VAX/VMS. Various parts available February - October 1988.

Contact: Rachel Rusting (617) 661-1480
Intermetrics, Inc.
7333 Concord Ave.
Cambridge, MA 02138

2.4.2 Mentor Graphics

Description: VHDL simulation environment. Available second quarter 1989

Contact: Rob Mendesdacosta (503) 626-1254
Mentor Graphics Corporation
8500 SW Creekside Place
Beaverton, OR 97005-7191

2.4.3 Microelectronics and Computer Technology Corp.

Description: VHDL analyzer and simulator. Available to members only.

Contact: Steve Grout (512) 338-3516
MCC CAD Program
Box 200195
Austin, TX 78720

2.4.4 Vantage Analysis

Description: VHDL analyzer and simulator for APOLLO workstation. Interfaced to Mentor software. Available November 1988.

Contact: B. La Porte (415) 659-0901

Vantage Analysis
42840 Christy St.
Freemont, CA 94538

2.4.5 View Logic Systems

Description: Subset VHDL analyzer and simulator for IBM PC/AT class computers. Available June 1988.

Contact: L. Asher (617) 480-0881
View Logic Systems
275 Boston Post Rd. W
Marlboro, MA 01752

2.4.6 Zycad

Description: VHDL analyzer and simulator for general Unix hosts and VAX/VMS interfaced to other analysis tools in the M.2 tool set. Available March 1989. Translator ISP' to VHDL available now.

Contact: George McCaskill (216) 229-8900 or (800) 545-8765
ZYCAD
1100 Cedar Ave.
Cleveland, OH 44106

2.4.7 Teradyne

Description: Read and write subset of structural and behavioral VHDL. Vanguard schematic capture will produce structural VHDL. AIDA and LASAR simulators will support VHDL.

Contact: Philip Odence (617) 482-2700
Teradyne, Inc.
321 Harrison Ave.
Boston, MA 02118

Hardware Accelerators

2.4.8 Zycad

Description: VHDL interface, at the structural level, to the Zycad accelerator.

Contact: Todd Oseth (201) 538 7833
Zycad
10 Madison Ave.
Morristown, NJ 07960

Synthesis

2.4.9 Honeywell Corporate Systems Development Division

Description: VHDL synthesis tool. Available September 1988.

Contact: Stan Krolikoski (612) 541-6843
Honeywell CSDD
1000 Boone Ave N
Golden Valley, MN 55427

2.4.10 JRS Research Laboratories

Description: VHDL synthesis to Seattle Silicon Concorde retargetable Ada to microcode compiler via VHDL model. Available March 1989.

VHDL models of VHSIC Phase 1 chips made by Texas Instruments, Honeywell, and TRW. Available September 1988.

Contact: Erwin Warshawsky (714) 972-2201
JRS Research Laboratories
1036 W. Taft Ave.
Orange, CA 92665-4121

2.4.11 Silc Technologies Inc.

Description: VHDL synthesis Tool. Available June 1989.

Contact: Lawrence Beecher (617) 273-1144
Silc Technologies Inc
34 Third Ave.
Burlington, MA 01803

2.4.12 Silicon Compiler Systems

Description: VHDL synthesis to compiled silicon and compiled silicon to VHDL. Available late 1989.

Contact: Kirk Lemon (408) 371-2900
Silicon Compiler Systems
2045 Hamilton Ave
San Jose California 95125

2.4.13 Trimeter Inc.

Description: Synthesis tool.

Contact: Henry Alward (503) 645-7039
Trimeter Technologies
15455 N. W. Greenbrier Parkway
Beaverton, OR 97006

Modeling

2.4.14 EIS Modeling, Inc.

Description: Various VHDL related services, including model development, application specific training, test, and verification of models. Available June 1988.

Contact: Gabe Moretti (415) 964-2296
EIS Modeling Inc.
2483 Old Middlefield Way, Suite 130
Mountain View, CA 94043

2.4.15 Logic Automation

Description: VHDL models of standard commercial parts.

Contact: James Morris (503) 690-6900
19500 N.W. Gibbs Drive
Beaverton, OR 97006

2.4.16 Quadtree Software Corporation

Description: VHDL models of electronic parts

Contact: Vicki Andrews (408) 436-3550
Quadtree Software Corporation
2020 North First Street, Suite 205
San Jose, CA 95131

Integration and Adaptation

2.4.17 CAD Language Systems

Description: VHDL training courses. Available January 1988. VHDL integration platform targeted to a wide variety of hosts and operating systems for integrating tools such as synthesizers, timing verifiers, and simulators. Available March 1988.

Contact: Mark Steffler (301) 424-9445
CAD Language Systems
51 Monroe St. Suite 606
Rockville, MD 20850-2419

2.4.18 Gateway Design Automation

Description: Translator for Verilog to VHDL available March 1989.
VHDL Analyzer simulator available in 1989.

Contact: Ronna Alintuck (508) 458-1900
Gateway Design Automation Corporation
Two Lowell Research Center Drive
Lowell, MA 01852-4995

2.4.19 GenRad Incorporated

Description: Translator for VHDL to/from HILO. Available March 89.
VHDL analyzer - simulator. Available in 1989.

Contact: Raymond F. McNulty (508) 369-4400 ext. 2970
Douglas S. Clauson (508) 369-4400 ext. 2862
GenRad, Inc.
300 Baker Ave.
Concord, MA 07142

2.4.20 Research Triangle Institute

Description: Translators for VHDL structure to schematic, schematic to VHDL structure, VHDL structure to EDIF 2.0, EDIF 2.0 to VHDL structure, VHDL to Genesil, Genesil to VHDL. Available November 1988.

Contact: Wayne Hansley (919) 541-6180
Research Triangle Institute
PO Box 12914
Research Triangle Park, NC 27709

2.4.21 Silvar-Lisco

Description: Translator for Helix to VHDL available December 1988. VHDL analyzer simulator available in 1989.

Contact: Silvar-Lisco (415) 324-0700
1080 Marsh Road
Menlo Park, CA 94025

2.4.22 Vista Technologies

Description: Interactive VHDL tutorial and editor for Sun workstations. Available in first quarter 1989.

Contact: S. Swamy (312) 640-4712
Vista Technologies
50 Gould Center
Rolling Meadows, IL 60004

CHAPTER 3

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CHAPTER 3 - VHSIC INDUSTRIAL BASE

It is evident from the system and technology insertion activities described in Chapter 2 that VHSIC is having a major impact on DoD system developments. Not only are new hardware components going into the new systems but the techniques for designing complex chips and subsystems are being increasingly automated in order to be able to handle the enormous amount of data required to design them accurately within reasonable time and cost limits. To support these activities, an increasing number of companies are providing products and services which meet VHSIC specifications for feature size, speed, throughput, and environmental hardness. The chips being produced, however, must be qualified for military use if they are to be used in military systems.

The following sections list some of the companies providing VHSIC products and services, the status of qualification of Phase 1 VHSIC chips, and some of the supporting test and evaluation work being carried out at DoD in-house facilities. Chapter 5 discusses in some detail further developments being carried out for both the hardware and software improvements in the industrial base, and in new qualification procedures aimed at decreasing the time and expense required to qualify complex VHSIC class devices.

3.1 INDUSTRIAL CAPABILITIES

3.1.1 General Electric Microelectronics Center

o Fabrication process:
- 1.25 micron bulk CMOS; DESC certified for wafer fabrication
- 1.25 micron SOS CMOS; prototype
- 1.25 micron SOS CMOS (radiation tolerant); prototype
- 1 micron bulk CMOS; under development
- 0.8 micron bulk CMOS; under development

o Devices for sale:
- Bulk CMOS gate arrays to 12.6K
- SOS CMOS 10K gate array
- SOS CMOS rad hard 64K RAM

o Form:
- Single chip packages (DIP, LCC, LLCC, CPGA)

o Services available:
- Design through production and testing

- Foundry using Genesil compiler

o Design capabilities:
- Standard cells, gate arrays, silicon compiler (Genesil), logic simulation, fault simulation, VALID/Mentor. Entry at schematic, netlist, or PG tape.

o Point of contact:
- Doug Blackley (919) 549-3167
  GE Microelectronics Center
  P. O. Box 13409
  Research Triangle Park, NC 27709-3049

3.1.2 Honeywell

o Fabrication processes:
- Bipolar CML, 1.2 micron
- CMOS 5V 1.2 micron
- Rad-hard CMOS 5V, 1.25 micron

o Devices for sale:
- Bipolar gate arrays; up to 12,000 gates
- Radiation-hardened static RAMs
- Electro-optical signal processing chip set

o Form:
- Single chip packages up to 284 pins and multichip packages
- Wafer form (for use in multichip packages)

o Design capabilities:
- Standard cell and gate array, libraries for CMOS, bipolar, and radiation hard circuit technologies.
- VHDL design interface available 1989
- Design interface available in 1989

o Points of contact:
- VHSIC products
  Lucien DeBacker (719) 540-3807
  Honeywell SSED
  1150 East Cheyenne Mountain Boulevard
  Colorado Springs, CO 80906

- VHSIC programs
  George Anderson (612) 541-2045
  Honeywell SSED
  12001 State Highway 55
  Plymouth, MN 55441

3.1.3 Hughes Microelectronics Centers - Carlsbad and Newport Beach

o Fabrication processes:
- 1.25 micron CMOS/SOS, 3.3 to 5.0 V, radiation hard
- 1.1 micron CMOS, radiation hardening in development

o Devices for sale:
- Multi-channel correlator
- Single channel correlator
- Signal tracking subsystem
- Configurable gate arrays

o Forms:
- Chip
- Single chip packages including PGA, LCC, LLCC, and quad flatpacks
- Multichip package

o Design capabilities:
- Standard cell, full custom, structured-custom cell, and gate array
- RAM, ROM, and PLA generators
- Mentor Graphics workstations
- Design entry from behavioral, RTL, or logic description

o Other Services
- Foundry service from CALMA tapes

o Point of contact:
- R. W. Dodge (619) 931-3196
  Hughes Microelectronics Center
  6155 El Camino Real
  Carlsbad, CA 92009

3.1.4 IBM

o Fabrication processes:
- 1.0 micron 5 V CMOS, DESC certified 12/11/87
- 1.0 micron 5 V rad hard CMOS
- 0.5 micron 3.3 V CMOS baseline
- 0.5 micron 3.3 V rad hard CMOS

o Devices for sale:
- Configurable Static RAM (CSR)
- Bus Interface Unit (BIU)
- Systolic Processor (SP)
- Address Generator (AG)
- Signal Processing Element (SPE)
- 64K, 256K radiation hardened SRAM; engineering sample
- Fourier transform module
- Generic VHSIC spaceborne computer chips - 2Q89
- Common signal processor chip set

o Form:
- Chip
- Single chip package
- Multi chip package

o Design capabilities:
- VHDL design capability 4Q89
- Custom, master image, gate array to 25K gates

o Other services
- Foundry

o Points of contact:
- Philip B. Johnson (703) 367-5547
  VHSIC Program Manager

- Jay Harford (703) 367-1041
  VHSIC Marketing
  IBM Federal Sysems
  9500 Godwin Drive
  Manassas, VA 22110

3.1.5 Intel Corporation

o Fabrication process:
- 1 micron, 5 volt CMOS; DESC certified to level B; QML certification scheduled for mid 1989

o Devices for sale:
- 51C98 64K SRAM 38510/613; currently available
- 80386 32 bit microprocessor; to be available late 1989

o Forms:
- 51C98: 22-lead ceramic DIP
- 80386: 168-lead fine pitch quad flatpack

o Other services offered:
- In-circuit emulator available for 80386

o Points of contact:
- Honore Bates (51C98) (602) 961-2970
- Barb Stoner (80386) (602) 961-8170
- Richard S. Walton (602) 961-2864
  (VHSIC Program Manager)
  Intel Corporation
  5000 W. Chandler Blvd., MS CH3-89
  Chandler, AZ 85226

3.1.6 LSI Logic Corporation

o Fabrication processes:
- CMOS 1.0 micron, 5 V

o Devices for sale:
- Gate arrays, 60, 80, 100K estimated gate capacity; DESC audit 02/22/88
- MIPS architecture 32-bit RISC processor with memory management
- MIPS architecture floating point processor
- 32-bit IEEE floating point processor
- 32-bit RISC CPU; available 3Q89
- Integrated floating point unit; available 3Q89

o Form:
- Chip
- Single-chip package

o Point of contact:
- Joe Ferro (408) 434-6422
  Manager, Strategic Military Programs
  LSI Logic Corporation
  1551 McCarthy Blvd.
  Milpitas, CA 95035

3.1.7 Motorola

o Fabrication process:
- 1.2 micron CMOS

o Devices for sale:
- 5 V CMOS gate arrays - 3K to 105K gates with RAM/ROM capability

o Form:
- Single chip package

o Design capabilities:
- Designs accessible through Mentor/Sun workstations at the schematic entry level
- Macrocell library supporting scan test design

o Point of contact:
- D. Fincher (602) 821-4483
  Motorola Inc.
  1300 N. Alma School Road
  Chandler, AZ 85224

3.1.8 National Semiconductor Corporation

o Fabrication processes:
- CMOS 1.2 micron 5 V; DESC certification 11/10/86

o Devices for sale:
- Gate arrays from 7.5K to 175K gates; release scheduled for 4Q89
- Standard cells up to 80K gates; available 2Q89

o Form:
- Packaged devices in standard DIP and surface mount forms

o Design capabilities:
- National DA4 design automation software
- VHDL simulation capability available as part of DA4
- Design entry from customer's CAD system or from Genesil compiler

o Point of contact:
- Ray Bortner (408) 721-7644
Marketing Manager, ASIC/VHSIC Military Products
National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA 95051

3.1.9 Raytheon Company

o Fabrication process:
- 1.25 micron, rad hard, 5.0 volt, CMOS

o Devices for sale:
- Gate arrays - 5K to 20K gate
- FPMAK: Floating point multiply/accumulate kernel

o Form:
- Chip
- Single chip package - PGA and LCC

o Design capabilities:
- Simulation, fault grading, routing, and ERC/DRC checking
- Built-in-test
- Integrated verified library for gate array and standard cell design

o Points of contact:
- Peter Goshgarian (Components)
Raytheon Company
Semiconductor Division
- Scott Stephen (Systems)
Raytheon Company
Microelectronics Center

350 Ellis Street
Mountain View, CA 94039
(415) 968-9211 X7828

358 Lowell Street
Andover, MA 01810
(508) 470-9000 X9114

3.1.10 Silicon Compiler Systems

o Fabrication processes supported:
- 1.25 and 1 micron 5V CMOS
- 1.25 micron rad hard 5V CMOS in 3Q89

o Foundries supported:
- GE MEC
- Harris
- Honeywell
- National Semiconductor
- NCR
- Performance Semiconductor
- VTC

o Products for sale/lease:
- Genesil IC design system for system engineers
- GDT IC design system for IC design engineers
- LSIM mixed-mode analog and digital simulator for simulation
- LogicCompiler option for logic synthesis
- ATG option for automatic test vector generation
- Rad-hard libraries available in 3Q89

o Design capabilities:
- Full custom chip design
- Mixed mode multi-level simulation
- Fault simulation
- Design for test
- VHDL descriptions of new designs

o Other services:
- Design tool training courses

o Points of contact:
- Jeff Elias (Genesil) (408) 371-2900
- Richard Gordon (GDT) (201) 580-0102
- Kirk Lemon (Military) (408) 371-2900

Silicon Compiler Systems
2045 Hamilton Avenue
San Jose, CA 95125

3.1.11 Texas Instruments

o Fabrication processes:
- CMOS 1.0 micron
- CMOS 0.8 micron
- BiCMOS 0.8 micron

o Devices for sale:
- 1.0 micron CMOS gate array family to 18K gates
- 1.0 micron CMOS standard cell family to 50K gates
- 1.0 micron CMOS digital signal processor family, 33 MFLOPS, 16 MIPS maximum throughput.

- 0.8 micron CMOS MIL-STD-1750A chipset, including:
  Data processor unit
  Memory management unit
  General logic unit
  Processor control interface
  Discrete input/output
  TMBUS interface unit
  PIBUS interface unit

o Form:
- Single chip packages: DIP, PGA, quad flatpack, gullwing

o Design capabilities:
- Custom ASIC's to 100K gates, standard ASIC (gate arrays or standard cells) using Daisy and Mentor workstations
- Silicon compiler design services
- Module design

o Points of contact:
- Robert F. Grimmer (Chips) (214) 480-1942
  Texas Instruments
  P.O. Box 660246 MS 3145
  Dallas, TX 75266

- Anthony J. Coumelis (Modules) (214) 575-3530
  Texas Instruments
  P.O. Box 869305 MS 8435
  Plano, TX 75086

3.1.12 TRW

o Fabrication processes:
- 1.25 micron, 5.0 V CMOS, radiation hardened
- 0.5 micron, 3.3 V CMOS, radiation hardened; in development

o Devices for sale:
- Window Addressable Memory
- Content Addressable Memory
- Address Generator; QPL in early 1989
- Microcontroller
- Matrix Switch
- Register Arithmetic Logic Unit
- Multiplier Accumulator
- Convolutional Decoder
- Convolver

o Form:
- Bare die (limited quantities for some designs)
- 132 pin JEDEC perimeter leaded

o VHDL capability:
- Accepts VHDL chip descriptions as point of entry data
- System/subsystem complete design

o Point of contact:
- T.A. Zimmerman (213) 814-2400
  TRW Electronic Systems Group
  One Space Park
  Redondo Beach, CA 90278

3.1.13 United Technologies Microelectronics Center

o Fabrication process:
- 1.2 micron rad-hard 5V CMOS; available 3Q89

o Devices for sale
  - 1.2 micron 20-50K rad-hard gate arrays; available 3Q89

o VHDL models available:
  - VHDL models available for cell library

o Form:
  - Chip
  - Single chip package

o Design capabilities:
  - Custom, standard cell, and gate array design services
  - Workstation and VAX-based design system supports design capture; logic, timing, and fault simulation; layout and test program generation.

o VHDL capability:
  - Circuit description output in VHDL

o Point of contact:
  - Ron Hehr (719) 594-8124
    Semicustom Product Line Manager
    United Technologies Microelectronics Center
    1575 Garden of the Gods Road
    Colorado Springs, CO 80907

3.1.14 VTC Incorporated

o Fabrication Processes:
  - CMOS 1.0 micron 5V

o Devices:
  - VME Bus interface, VIC068
  - 1.0 micron foundry services on the Genesil silicon compiler.

o Form:
  - 144 Pin PGA

o Point of contact:
- Marc Ostrowski (612) 851-5238
  VTC Incorporated
  2401 East 86th Street
  Bloomington, MN 55425-2702

3.1.15 Westinghouse - Advanced Technology Division and Chesapeake Group

o Fabrication processes:
- CMOS 1.25 micron, radiation hard, 5V and 3.3V
  Qualification of 54K gate array family planned by 1Q90

o Devices for sale:
- Gate array family - 10K to 54K gates

o Form:
- Chip
- Single chip packages - DIP, PGA, LCC, quad flat packs

o Design facility:
- Gate array routing from Daisy, CAE/Tektronix or Mentor net list
- Masks made from CALMA database

o Point of contact:
- Richard C. Lyman (301) 765-2379
  Westinghouse Advanced Technology Division
  P. O. Box 1521
  Mail Stop 3A13
  Linthicum, MD 21203

3.2 QUALIFICATION OF VHSIC DEVICES

3.2.1 Status Overview

The qualification of integrated circuits for military use (JAN qualification) requires a number of distinct steps: (1) characterization and documentation of the device in a dated specification (called a "slash sheet") in accord with MIL-M-38510, (2) certification of the production line to assure a controlled manufacturing process in accord with MIL-STD-976, and (3) testing of a designated production lot in accordance with MIL-M-38510 and MIL-STD-

883C procedures. A manufacturer must certify both the fabrication and assembly process before the device can be considered for the QPL. The following tables show the status of these procedures for those manufacturers participating in the production of VHSIC devices.

Specification Status

Company	Device	Tech	Slash Sheet/version	Date
NSC	SRAM 64K	CMOS	MIL-M-38510/610	02/25/87
Intel	64KSRAM	CMOS	MIL-M-38510/613	05/12/87
Motorola	4PM	CMOS	MIL-M-38510/615	11/24/87
TRW	AG	3D-STL/CML	MIL-M-38510/616	11/24/87
GE	FFT	CMOS	MIL-M-38510/630	12/11/87
IBM	SPE	CMOS	MIL-M-38510/620	12/21/87
Honeywell	HC20K	CMOS	MIL-M-38510/605 (1)	02/27/87
Westinghouse		CMOS	MIL-M-38510/605	02/27/87

(1) MIL-M-38510/605 is a generic CMOS gate array family.

VHSIC Fabrication Certification

Company	Technology	Location	Date	Status
National 64K	CMOS	Santa Clara (VLSI)	11/10/86	Certified
TRW	3D	San Diego (LSIP)	03/06/87	Certified
GE	CMOS	(AVLSI)	04/17/87	Certified
IBM	CMOS	Manassas (VLSI)	08/11/87	Certified
Intel	CMOS	Aloha, OR (FAB5)	12/17/87	Certified
Honeywell	CML	Col Spr ADB1(FAB1)	10/87	DESC audit
Honeywell	CMOS	Col Spr CMOS3 (FAB3)	08/88	DESC audit

VHSIC Assembly Certification

Company	Location	Date	Status
IBM	Manassas, VA	12/03/86	Certified
TRW	Redondo Beach, CA (MEC)	03/06/97	Certified
GE	Research Triangle Park, NC	04/17/87	Certified
IBM	Manassas, VA	08/11/87	Certified
Intel	Chandler, AZ	12/17/87	Certified
National 64K	Tucson, AZ (MilPro)	03/24/88	Certified
Honeywell	Colorado Springs	10/87	DESC audit

Device Qualification Status

Company	Device	MIL-M-38510/	Status	QPL
Intel	64K SRAM	613	Complete	05/12/88
IBM	SPE	620	Qual lots at assembly	06/89 (est)
TRW	AG	616	Qual lots in assembly	06/89 (est)
NSC	SRAM 64K	610	Qual lots in assembly	
GE	FFT	630	Qual lots in assembly	06/89 (est)

3.2.2 New Starts 1988: Westinghouse (Advanced Technology Division)

- o USAF contract effort on generic qualification of VHSIC gate array family to MIL-M-38510/605A started September 1988.
- o Gate array family is 1.25 micron (0.9 eff), 5V and 3.3V CMOS; consists of 54K, 28K, 20K, 10K, 4K and 3K gate arrays.
- o Process monitor design submitted 4Q88.
- o DESC audit of VHSIC gate array wafer fabrication and assembly line planned for 3Q89, generic qualification planned by 1Q90.

The USAF contract support will result in the availability of JAN qualified VHSIC CMOS 1.25 micron (0.9 eff) gate arrays early in 1990. New gate array designs can be prototyped in ten days after generation of the e-beam personalization tapes. When QPL status is realized, new JAN gate arrays will be available in less than four weeks, because the usual JAN qualification requirement will have been met by the generic gate array family qualification. This fast turn around capability will benefit defense programs at Westinghouse and will be available to other DoD programs. The gate array family will be available to other DoD suppliers through The Chesapeake Group, a Division of Westinghouse.

3.3 TEST AND EVALUATION

3.3.1 Army In-House Test and Evaluation

The Electronics Technology and Devices Laboratory (ETDL) continued the investigation of hot electron effects in submicron transistors. A total of 672 IBM transistors were packaged for a long term hot electron study. The devices, with submicron geometries and normal operating voltages of +3.3 volts, were stressed with +3.6, +3.9, +4.2, and +4.5 volts at -55°C for over 100 hours. The devices stressed at +4.2 volts exhibited minor degradation. Those stressed at +3.6 and +3.9 volts did not measurably degrade. The devices stressed at +4.5 volts showed a drastic degradation in V_t, $I_{dds,}$ and g_m which saturated quickly over time. Subsequent analysis determined the cause to be electron trapping in the gate oxide and generation of interface states at the Si-SiO_2 interface. These results were confirmed by IBM and detailed in a paper presented by ETDL at GOMAC-88. See reference 3.1.

LSI Logic, Inc. used a 1.25 micron CMOS 70,000 gate array (with 25,000 usable gates) to fabricate an arithmetic element controller (AEC) which has been functionally tested and verified at ET&DL. The device has been designed for a VHSIC upgrade of the Firefinder radar (see Chapter 2, Section 2.2.1.4). Using ETDL's TOPAZ tester, the maximum functional speed measured over the military temperature range versus the design goal was:

Arithmetic Element Controller (AEC)

Temperature (°C)	Speed (MHz)	Design Goal (MHz)
25	33	35
-55	34	35
125	25	17

The IBM 1.0 micron CMOS Special Processing Element (SPC) has also been functionally tested at ETDL. Initial results are:

Special Processing Element (SPE)

Temperature (°C)	Speed (MHz)	Design Goal (MHz)
25	27	25
-55	26	25
125	20	25

Functional testing of the IBM VBIU has been initiated. The TOPAZ device under test (DUT) board has been fabricated and debugged. Preliminary tests of the VBIU indicated 50 MHz operation.

3.3.2 Navy In-House Test and Evaluation

The Naval Research Laboratory (NRL) Signal Processing Staff (Code 5305) previously reported on developing a physical model of the TRW VHSIC MAC chip on their Daisy PMX system in order to design, simulate, and program a VHSIC Sidelobe Canceler board. The VHSIC gate arrays were fabricated by Motorola and delivered to NRL. See reference 1.2, "VHSIC Annual Report for 1987".

The delivered gate arrays were tested on the Daisy PMX system as real chips, and compared with the models already entered into the system. Since the models and the actual devices performed identically, they were installed on the already prepared boards along with the TRW MAC chips. The boards run as designed, and have been used with simulated data at speeds up to 19 MHz. They are now being connected to an A/D system for processing of actual radar data.

In addition, NRL has been installing and verifying the readability of the TRW VHDL Macrocell descriptions of their superchip. The descriptions will be run on a SUN VHDL system using the test vector tapes to be provided in VHDL by TRW. Several cells have been compiled, but the descriptions were too large to run on the VMS MicroVAX. This effort will continue in 1989.

3.3.3 Air Force In-House Test and Evaluation

General. During FY88, the Microelectronics Reliability Division at the Rome Air Development Center performed detailed tests and evaluations of VHSIC devices. The RADC facility houses the baseline VHSIC electrical test system, the TISSS central host computer, a

VLSI design workstation, and a scanning electron microscope.

Test program development and device characterization focused on the Intel VHSIC static RAM, MIL-M-38510/613. This was the first VHSIC device to receive military qualification status. The characterization included all ac, dc, and functional tests included in MIL-M-38510/613, along with three-dimensional shmoo plots of various operating characteristics. The testing performed on the samples obtained by RADC indicated that the devices were able to meet all specification limits by wide margins.

Packaged VHSIC Devices. During FY88, the RADC Microelectronic Reliability Division performed detailed tests and evaluations of VHSIC devices produced under the DoD VHSIC program. Packaged devices were subjected to tests contained in MIL-STD-883 (Test Methods and Procedures for Microelectronics). This effort is directed towards assessing the package construction and packaging processes of the VHSIC contractors to establish the suitability of these packaged devices for qualification to military standards. The result of this evaluation is a Product Evaluation Report (P.E.) that is first shared with the manufacturer to help in improving its processes and then forwarded to the DoD VHSIC Program Office to advise of the contractor's progress toward achieving a qualifiable product. In addition to the six primary VHSIC contractors (Honeywell, Hughes, IBM, Texas Instruments, TRW, and Westinghouse), this program will also review VHSIC parts from other companies such as General Electric, Raytheon, Harris, Intel, and Motorola.

VHSIC package evaluations completed in FY88 at RADC/RBRE on packaged engineering samples of devices are as follows.

Honeywell

- o Arithmetic processor (AP) - 180 I/O pin grid array (PGA)
- o Tape automated bonded (TAB) C-fired ceramic package

TRW

- o Address generator (AG) - 128 lead top-brazed quad flat pack
- o Register arithmetic logic unit (RALU) - 128 lead top-brazed quad flat pack

Westinghouse

- o 64 Static random access memory - 40 lead dual-in-line side brazed solder sealed package
- o 16K SRAM - 40 lead dual-in-line side brazed solder sealed package
- o Gate arrays - 224 I/O PGA

IBM

- o Complex multiply & accumulate (CMAC) - 240 I/O PGA multilayer ceramic package
- o Single chip packages - 220 lead - contained the C/4 thermal test chip.

Texas Instruments

- o Multi-path switch (MPS) - 84 I/O leadless ceramic chip carrier (LCCC)
- o Array controller sequencer (ACS) - 84 I/O LCCC
- o Static random access memory (SRAM) - 32 I/O LCCC
- o Data processing unit (DPU) - 84 I/O LCCC
- o General buffer unit (GBU) - 84 I/O LCCC
- o Vector arithmetic logic unit (VALU) - 164 I/O open via chip carrier (OVCC)

Intel

- o 64K SRAM - 22 lead side brazed 300 mil package - This packaged device has been granted QPL status by DESC. Devices received at RADC were electrically functional. They will be put through a full device qualification procedure and results supplied to Intel.

All of the above devices/packages were subjected to the routine MIL-STD-883 analytical examinations in RADC's Product Evaluation Laboratories.

As a result of these package evaluations, a number of potential reliability problem areas were detected. Results of individual analysis were provided the specific contractors for corrective action. Typical problems uncovered were: lid seal and pin corrosion, damage to external components and adhesion problems between Cu leads and polyimide supports, hermeticity failures, high moisture content in sealed packages, PIND failures (internal particles), bond strength failures (e. g. less than minimum strength for wire diameter used), presence of large voids in die attach material (which could present heat dissipation problems), surface defects of die including scratches and cracks, and poor bond placement on pad area.

The results of these 1988 evaluations will be documented in a final report. Package evaluations will continue on updated packaging technology. See references 3.2 and 3.3.

CHAPTER 4

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CHAPTER 4 - PHASE 2: SUBMICRON TECHNOLOGY

4.1 TECHNOLOGY GOALS AND APPROACHES

In October 1984, Phase 2 contracts were awarded to Honeywell, IBM, and TRW for the development of the second generation of VHSIC technology which would require new tools, new techniques, and more aggressive technical approaches. The VHSIC Program Office required that this new IC technology meet, among other requirements, the following specifications:

Feature size	0.5 micron
Functional throughput rate	10^{13} gate-Hz/cm^2
On-chip clock rate	100 MHz
Failure rate	0.006%/1000 hours
Radiation (total dose)	$5x10^4$ rad(Si)
Built-in fault detection	>95% coverage single "stuck-at" faults
	>75% coverage CMOS "stuck-open" faults
Interoperability	PI bus and TM or ETM bus

The specific tasks which the contractors have been engaged in for the past four years are grouped into eight major areas:

(1) chip technology and fabrication,
(2) system architecture design,
(3) chip design,
(4) support software,
(5) interoperability (BIU) design,
(6) module design, fabrication, and demonstration,
(7) brassboard design and fabrication (option),
(8) design and simulation methodology.

The progress and current status of each of the contractors is separately described below. More detailed information can be obtained from the interim Phase 2 technical reports which are listed as references 4.1 through 4.21.

4.2 HONEYWELL

The approach taken by Honeywell to produce and demonstrate 0.5 micron VHSIC chips operating in a brassboard module is to design two large configurable gate arrays which are then used to design and fabricate three 0.5 micron chips. The characteristics of the two generic gate arrays are shown in the table below.

Submicron Gate Array Characteristics

	HM35000	HM70000
Chip size (mils)	280 x 280	360 x 380
No. of Sectors	4	6
Gate array cells/sector	1728	2304
Pad layout	Double pad row	Double pad row
No. of pads	184	256
I/O	120	190
Chips per 4" wafer	80	43
Custom options	None	4K RAM w/two 16 x 16 register files Four 1K RAMs Six 16 x 16 register files 16 x 16 multiplier
Brassboard chips	BIU	APC, APU

Using these configurable gate arrays, the three submicron VHSIC chips are formed by customizing the metal interconnect layers of each to perform the functions of an electro-optical image processor similar to the one designed by Honeywell for the VHSIC Phase 1 program but with much higher speed and capability. The three VHSIC Phase 2 chips are a bus interface unit (BIU) for interoperability between modules, an array processing unit (APU) to do the basic arithmetic computations, and an array process controller (APC) to provide the control functions. Honeywell has designed a brassboard module to demonstrate these operations of the three chips.

The characteristics of the three VHSIC submicron chips are shown in the table below. The additional functions such as memory interfacing and input/output control are provided with 1.25 micron chips being designed on a commercial Honeywell 10,000 gate array.

BIU / APC / APU Chip Statistics

	BIU	APC	APU
Size (mm x mm)	7.0 x 7.1	9.23 x 9.57	9.23 x 9.57
Number of devices	74000	191433	233353
Equivalent gates	18K	26K plus 4K RAM	31K plus 8K RAM
I/O signals	103	190	190
Gate array cells used	3671	5458	5699
Cell utilization	53%	59%	82%
Chip power (135°C)	3.4 W	5.0 W	5.4 W
Test coverage (%)	>99.8	>99.8	>99.8

During 1988, the following accomplishments were achieved:

- The BIU was successfully designed and fabricated on the HM35000 gate array. The design proved to be fully functional on the first pass. Seven good BIU die were obtained from two of the eight wafers in the lot.

- The designs of the APC and APU chips were completed. These chips are larger than the BIU and must be fabricated on the larger HM70000 gate array.

- The Honeywell 0.5 micron chip set was selected by General Dynamics for use in the design and demonstration of an advanced cruise missile guidance system. The chip set, with the addition of a test bus interface chip, are to be supplied to GD after the VHSIC Phase 2 demonstration in late 1989.

- Under a subcontract with Honeywell, Motorola demonstrated the feasibility of establishing a second source for the 0.5 micron process, and the task was terminated.

Process technology: The Honeywell 0.5 micron process technology is based on bipolar transistors. Electron beam lithography is used for the critical dimension layers. Isolation grooves are formed around each transistor to reduce current leakage and make it possible to achieve a very high device packing density. There are four layers of metal interconnections with a 1.5 micron pitch (line plus space) at the first metal layer. During 1988, the processing of the metalization layers received the major attention. The first and second layers of metal are now patterned with optical lithography rather than with the e-beam machine in order to improve yield and wafer throughput. This change proved to be an appropriate strategy when, in July/June 1988, the processing steps were sufficiently consistent to successfully produce the

first functional BIU chips.

The primary effort of the program then shifted to the final design and fabrication of the larger HM70000 gate array. The gate arrays are used as their own test structures with specially designed test metal patterns and device designs to serve as process evaluators and monitors during the process development and de-bug stages which were underway during the latter half of the year. These test wafers are being processed to complete the four-layer metalization system with full dielectric interlayer thickness and a compatible CVD tungsten interlayer connection scheme.

In addition to the specific work on the metal interconnection layers, Honeywell identified the following major yield inhibitors and carried out a major effort to reduce them:

- o particulates in the processing equipments
- o interlayer dielectric leakage
- o collector-emitter current leakage
- o metal shorts
- o lithographic rework

Design. Honeywell completely verified the BIU chip design in silicon. In September, the good BIU chips passed 70 functional test vector sets (6063 vectors) and twelve (out of twelve) scan-path tests.

The structural design verification of the APC and APU chips was completed using the same test vectors used by the system designers to verify their functional design. After place and route and performance optimization, the critical paths were all determined to be under 20 nsec (greater than 50 MHz instruction rate, 100 MHz clock). The floorplan of the APU chip is shown in Figure 4.1.

The first runs of the APC and APU test wafers were completed in late September. The primary purpose of the test wafers is to check the custom circuits that were designed for the APC and APU chips. Initial wafer testing verified the design of all of the custom circuits including the register files, the 16 x 16 multiplier, and the 1K and 4K RAM circuitry. At year end, HM70000 test wafers results were sufficiently good that initial fabrication lots of the full product wafers were scheduled for January 1989.

The writable control store interface (WCSI) chip and the RAM interface (RAMIF) chips are being built on the Honeywell 1.2 micron bipolar HM10000 gate array. The interface chips provide logic level conversion and data pipelining between external memory and the submicron processor units. The logic level conversion was chosen to be compatible with CMOS TTL in order to conserve power and to conform to the General Dynamics design of the advanced guidance system.

APU CHIP FLOORPLAN

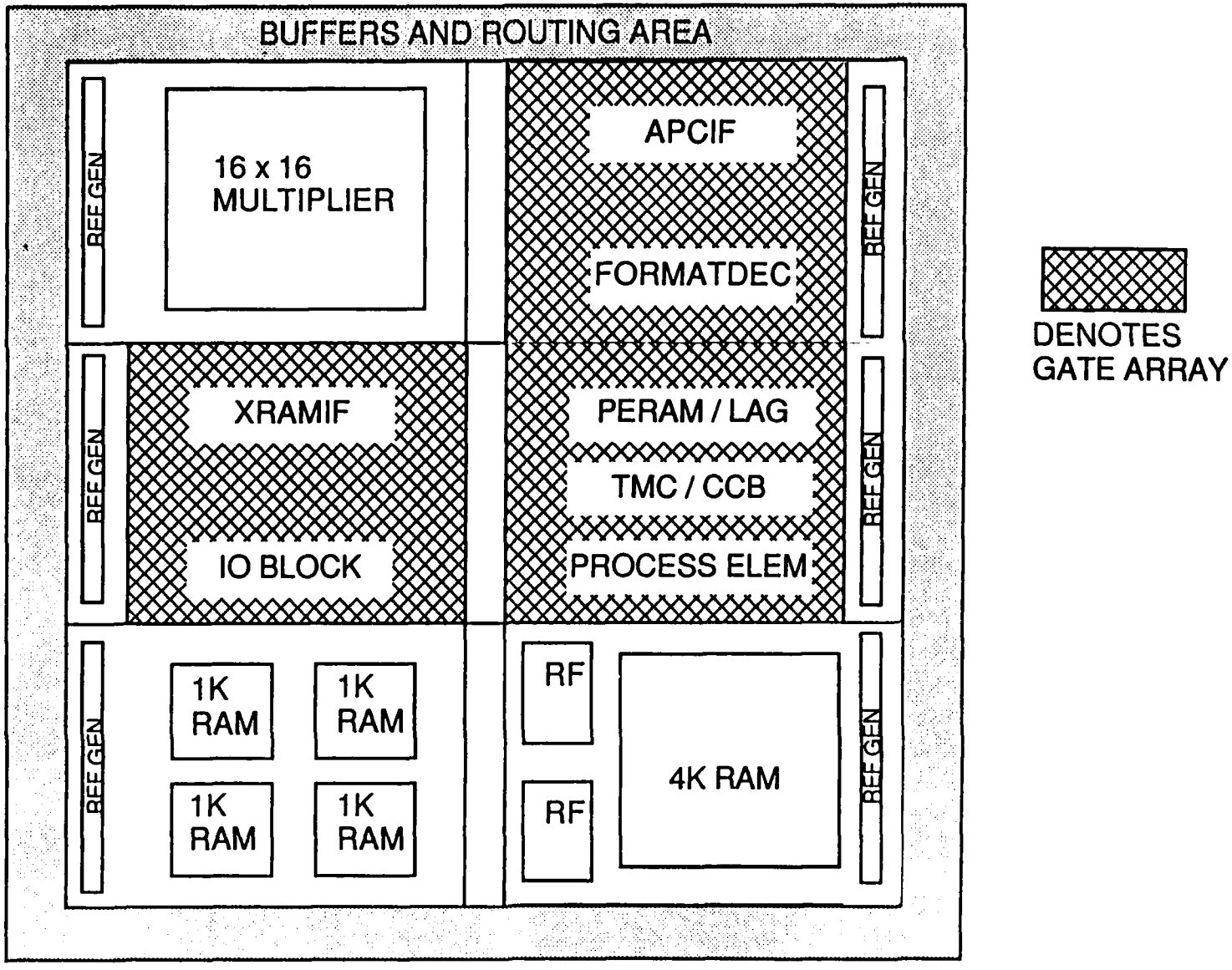


Figure 4.1 - APU Chip Floorplan

Packaging. Honeywell is developing both a single chip package and a multichip package for the Phase 2 chips. The single chip package is designed for 256 I/O pads arranged in a double row with an effective pitch of 5 mils at the chip periphery.

The design of the substrate for the brassboard multichip package (MCP) was completed, specifications were written, and substrates were ordered for thin-film multilayer processing. A preliminary routing of the signal layers was done as part of the design. The MCP can be routed in the two allotted signal layers within the substrate structure. In processing the substrate and mounting test chips in the packages, the results showed that the quality of the substrate was the most important determinant of yield. Therefore much of the effort during the year was spent developing a source of acceptable ceramic substrate material. An acceptable vendor with a superior co-fired ceramic has been identified and has supplied Honeywell with a large sample of lapped material. Yield studies and pinhole measurements on the substrates have begun. The features of the multichip package and the chip layout for the demonstration module are shown in Figures 4.2 and 4.3.

EOSP CML Chip Set: As part of the Phase 2 submicron program, Honeywell is also completing the migration of a 1.25 micron electro-optical signal processor chip set to CML bipolar technology. The functional design of the chip set is the same as that of the chip set designed by Honeywell for Phase 1. However, a standard cell design methodology has been developed and used for the two chips comprising the new chip set -- a parallel pipelined processor and a controller. The controller chip design has been successfully fabricated and verified as fully functional. The finished, packaged chip is shown in Figure 4.4. It operates at greater than 60 MHz from -55°C to +125°C. The PPP chip logic has been verified in silicon also but an I/O RAM functional block has not yet been shown to be fully functional.

The controller chip design is being thoroughly evaluated. When that is completed the chip will go into full reliability testing and characterization. The PPP will go through the same steps after it has been verified.

E-O Brassboard Demonstration. The architecture of the brassboard module that is being assembled to demonstrate the submicron chips is shown in Figure 4 5. The brassboard support system was verified by demonstrating an image passing operation . th all components of the support system functioning together under control of the module software and command interpreter.

The functional design of the Phase 2 chip set has been completed. Only documentation and test vector generation for the APU remain to be completed in the system chip design tasks.

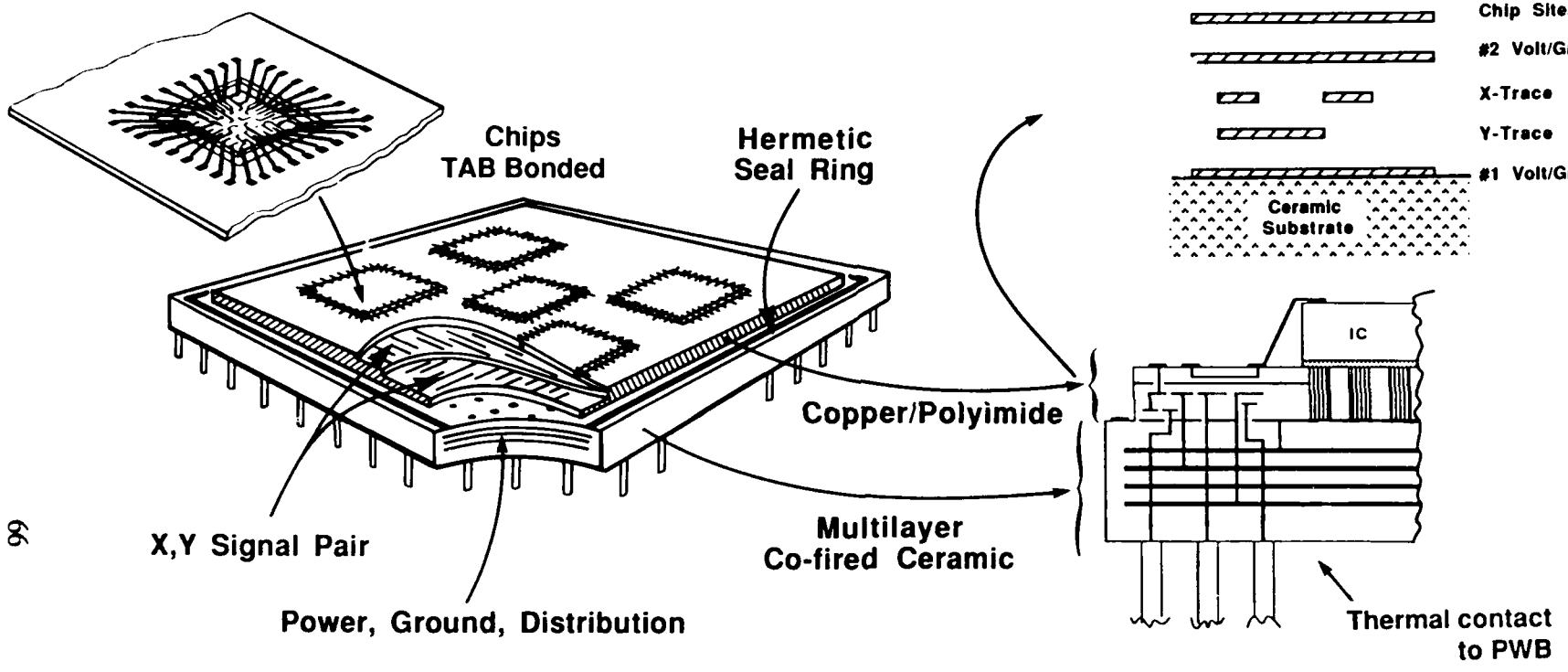
Plans: During 1989, the APC, APU, and interface chips will be fabricated so that the full brassboard module can be assembled and demonstrated. The emphasis will be put on completing and stabilizing the chip fabrication process steps -- especially the metalization systems. With good yield on the metal layers and the via interconnections, the dielectric layers

VHSIC SUBMICRON

Multichip Package Development

Honeywell

Brassboard MCP



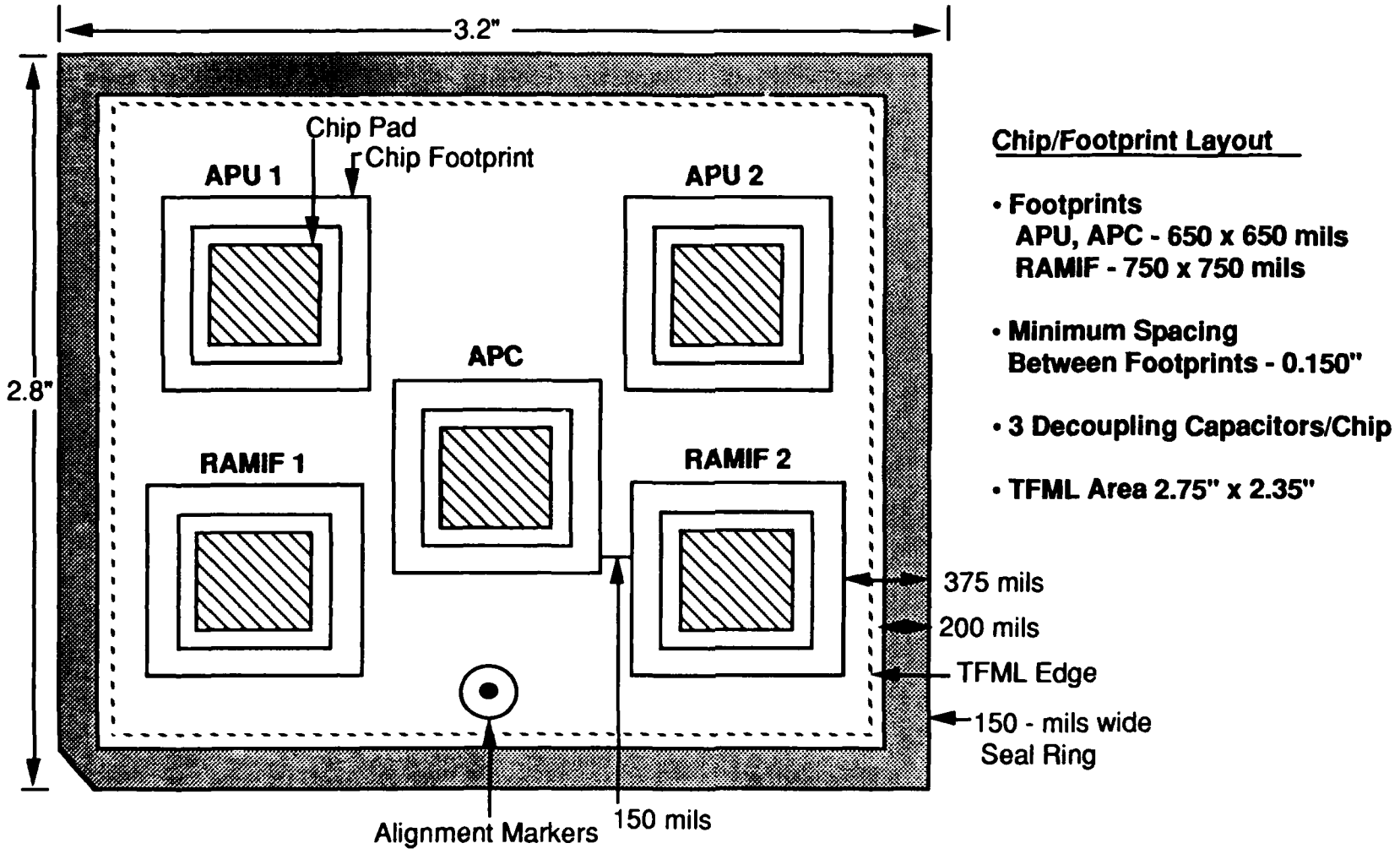
Cu/PI Structure

Features

- 5 VHSIC Chips (3 Types)
- 5 Copper Layers in Cu/PI
  - 1 Bonding Layer
  - 2 Voltage Planes
  - 2 Signal Planes
- 3 Tungsten Layers in Ceramic Substrate
  - 2 Power Planes
  - 1 Redistribution Layer
- 50 Ohm Offset Stripline
- Constant Impedance Structure
- 100 mil PGA, 539 Pins
- 1 mil Wide Lines, 5 mil Pitch
- 2.8" x 2.4" Active Area
- 3.2" x 2.8" Overall Area

71519

Figure 4.2 - Multi-chip Package



Chip/Footprint Layout

- **Footprints**
  APU, APC - 650 x 650 mils
  RAMIF - 750 x 750 mils
- **Minimum Spacing**
  Between Footprints - 0.150"
- **3 Decoupling Capacitors/Chip**
- **TFML Area 2.75" x 2.35"**

Figure 4.3 - Multi-chip Package Layout

Brassboard Module Architecture

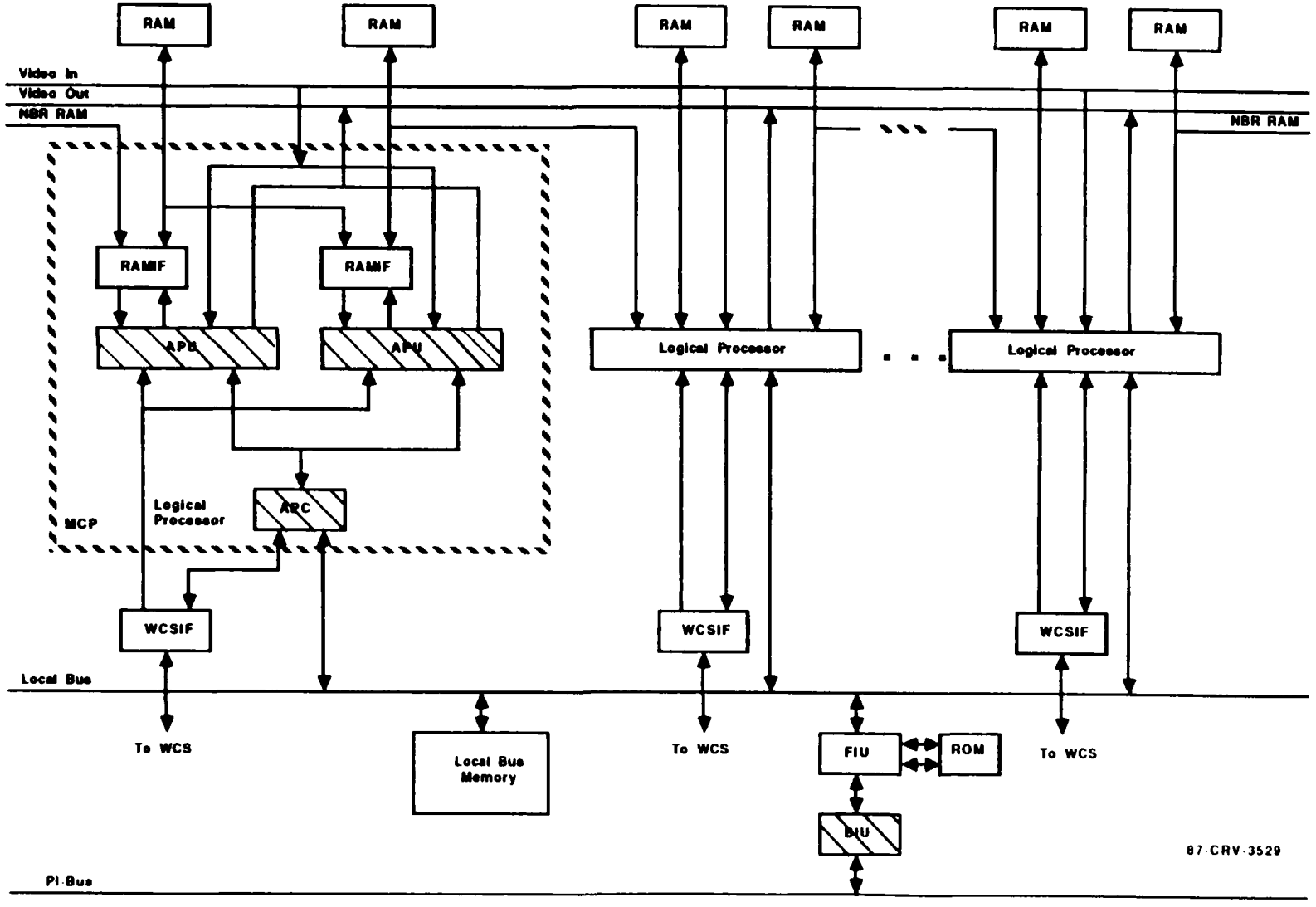


Figure 4.4 - Honeywell Brassboard Module Architecture

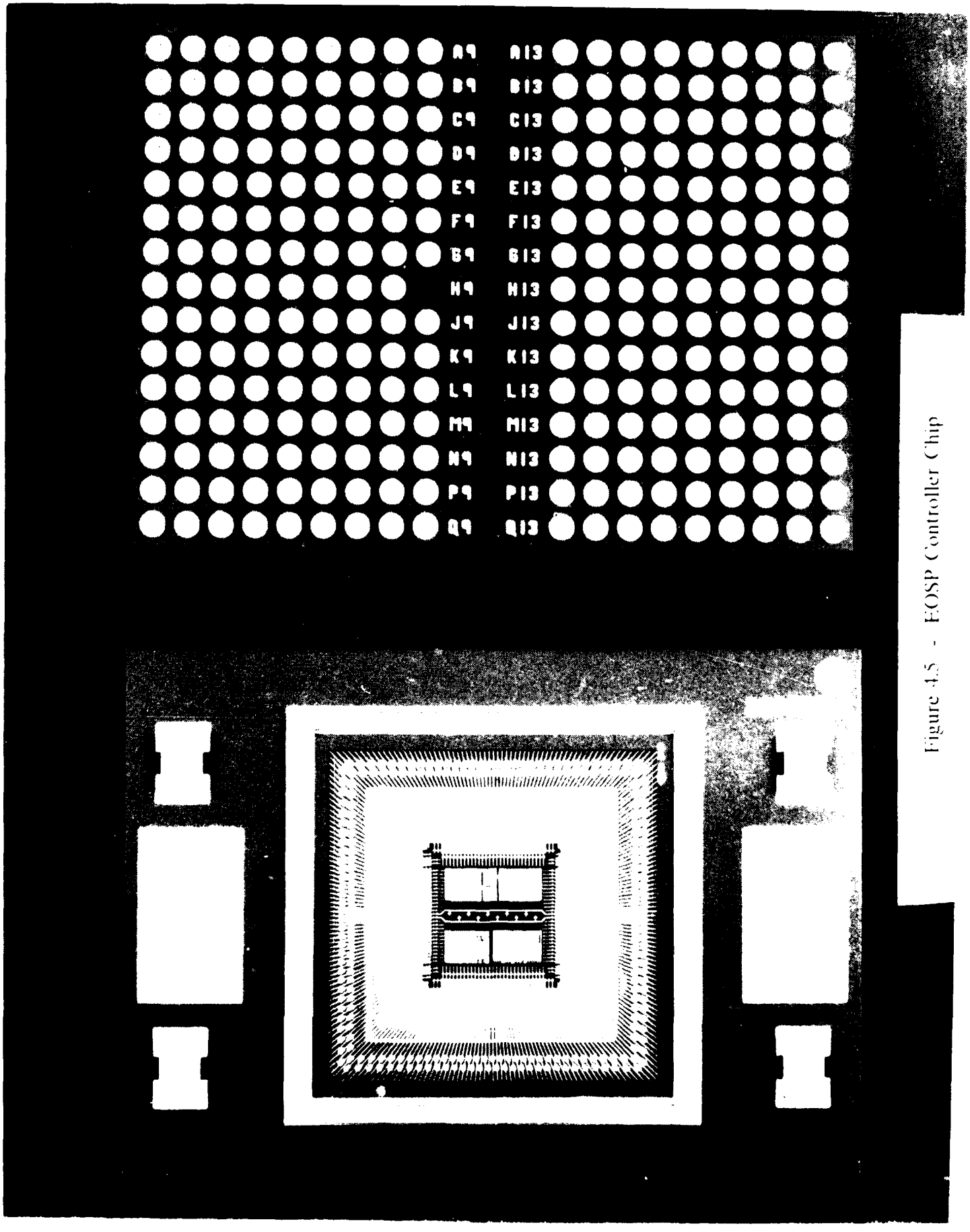


Figure 4.5 - EOSP Controller Chip

can then be increased in thickness in order to meet the speed requirements. The designs of all the chips will be documented as will the design automation techniques developed under the program.

Interim technical reports for Honeywell are listed as references 4.1 through 4.7.

4.3 IBM

During 1988, IBM successfully completed development of the 0.5 micron chip fabrication process, produced the four 0.5 micron chip types at excellent yield, and used them to assemble and demonstrate, on December 1, an acoustic beamformer brassboard module with 20 times the signal throughput of current operational equipment. These activities completed on schedule the requirements initially set out for the VHSIC Phase 2 program. Specific accomplishments during 1988 included:

- o Demonstration of the VHSIC bus interface unit (VBIU) and the systolic processor (SP) operating with 100 MHz on-chip clock rates.

- o The use, on the brassboard, of two multi-chip packages, each containing 16 VHSIC chips, both mounted on a single SEM-D circuit board. The 16 chip package provides very high chip (and hence functional) density with a 50 MHz chip-to-chip I/O rate within the package.

- o Achievement of the VHSIC radiation hardness goal of $2x10^5$ rad(Si) with no significant increase in the complexity of the fabrication process.

- o Production of the 0.5 micron chips with lot yields ranging from 5% to 30% depending on chip complexity, and an average yield of approximately 15%.

During 1989, IBM will continue work on two tasks. The first is to develop the full radiation hardness potential of the 0.5 micron process and the second is to demonstrate generic qualification procedures for an 0.5 micron manufacturing environment.

Interim technical reports for IBM are listed as references 4.8 through 4.14.

Processing Technology: The IBM process technology activity in 1988 was focused on achieving the required device performance and radiation hardness at high yield, and manufacturing the four deliverable chip types for use in assembling the brassboard.

Key features of the IBM process that support high device performance include 0.5 micron feature size polysilicon transistor gates, thin gate oxide, and self aligned titanium silicide (salicide) processing. High circuit density is achieved through the use of two wiring

levels of aluminum/copper plus a third metal layer for pads. High chip I/O count is achieved with a 21 x 21 area array of chip to substrate solder connections. These controlled, collapsible, chip connections (C4) provide direct attachment of the chip to single and multiple chip packages. The lithography process includes electron beam patterning for the 0.5 micron features. However, IBM also demonstrated, in 1988, the use of the Advanced Wafer Imaging System (AWIS), for fabricating 0.5 micron feature size devices with a completely optical lithography system.

IBM adopted the goal of merging the enhanced radiation and basic processes into a single process. The objective was to achieve the VHSIC Phase 2 radiation hardness goals without increasing the complexity or reducing performance and yield. This goal was successfully demonstrated in 1988. The result is a single VHSIC Phase 2 process that supports all applications. There is no cost or performance penalty for radiation hardened parts.

Twelve lots of the VHSIC Phase 2 chips (three for each of the four chip types) were fabricated in early 1988. Each of these lots was split. Half the lot was fabricated in the base process and half was fabricated in the enhanced process. The results showed excellent yields of fully functional parts. There was no noticeable difference in the yield or performance of baseline and enhanced chips. Subsequent reliability testing has shown no degradation in reliability of chips fabricated with the enhanced process.

Design: IBM has designed four chip types for the VHSIC Phase 2 program, the address generator (AG), the configurable static RAM (CSR), the systolic processor (SP), and the VHSIC bus interface unit (VBIU). The characteristics of the chip set are summarized in the table below. The chip designs were completed in 1986 and 1987. More than 3000 fully functional 0.5 micron VHSIC chips have been produced from these initial lots.

Each chip type has been tested functionally from room temperature to +125°C. The VBIU and SP have demonstrated 100 MHz on-chip logic at worst case temperature and ±5% voltage. The chips pass all functional tests and meet the VHSIC Phase 2 requirements. Each of the chip designs has been documented in the VHSIC Hardware Description Language. These parts are available for evaluation in brassboard and other applications. There are functional and electrical specifications available as well as the VHDL documentation.

Because of the excellent yield results from the first lots at 0.5 micron, IBM began fabricating five additional chip designs in the 0.5 micron process at no additional cost to the program. These chips are being fabricated in an all optical 0.5 micron process to evaluate the process and to further demonstrate the effectiveness of the 1.0 to 0.5 micron design migration strategy. The chips are the signal processing element (SPE) and a four chip 1750A CPU set that was designed in 1.0 micron for the Air Force generic VHSIC spaceborne computer program. These chips will be evaluated early in 1989.

IBM VHSIC Chip Characteristics

	CSR	SP	VBIU	AG
Chip size	5.5 mm	5.5 mm	5.5 mm	5.5 mm
Type	MI	Custom	MI	MI
No. of devices	144,000	80,000	36,400	48,000
Equivalent gates	9,200	33,000	15,000	24,400
	+18,000 RAM bits			
Power	680 mW	900 mW	850 mW	600 mW
No. of I/O	134	178	152	179
Cell utilization	95%	N/A	96%	92%
Test coverage	99.01%	99.22%	98.58%	99.35%
No. of connections	2,451	17,280	6,676	3,735
No. of vias	5,947	35,849	13,857	9,275
Length of M1 & M2 (Global wires)	2.00 m	7.0 m	3.56 m	2.69 m

Packaging: IBM has developed single chip and multi-chip packages (SCP and MCP) for the VHSIC Phase 2 program both of which feature the IBM flip-chip, direct attachment technique. The single chip package is surface mounted with 220 gullwing leads and internal decoupling capacitors. The package dimensions are 1.5" x 1.5" x 0.15". The lead pitch is .025". The thermal impedance is 6°C/watt from chip junction to the interconnect board. The package supports simultaneous switching of 64 I/O at 25 MHz from -55° to +125°C.

The multi-chip package can include up to 16 VHSIC chips and decoupling capacitors in a single package measuring 64 mm on a side. The 625 I/O leads are arranged in a pin grid array. The maximum chip-to-chip I/O rate over the temperature range of -55° to +125°C is 50 MHz. Repair procedures have been developed to replace defective chips on the package substrate. Both the single and multiple chip packages have passed all of the MIL-STD-883 qualification tests as summarized in the following accompanying table.

Test	Conditions	Results
Mechanical shock	1500 g (X and Z axes)	Passed
Vibration		
Sweep	5-2000 Hz, 20 g	Passed
Random	5-500 Hz, 0.04 g^2/Hz	Passed
Thermal cycle	-55° to 125°C @ 3 hours	Passed, 1800 cycles
High temperature storage	1000 hours @ 150°C	Passed
Constant acceleration	500 g, 1 minute	Passed
Moisture resistance		Passed
Salt atmosphere	24 hours (minimum)	Passed
Internal gas analysis	<5000 ppm H_2O	Passed

Brassboard Applications: The IBM brassboard is a sonar acoustic beamformer module intended for use in submarine systems. It contains two multi-chip packages with a total of 32 VHSIC chips mounted on a single SEM Format D card. A schematic diagram of the module layout is shown in Figure 4.6. It has been populated with 0.5 micron chips, fully tested, and was successfully demonstrated performing the beamformer function at 50MHz. This brassboard beamformer provides 20 times the throughput of the current AN/BSY-1 sonar beamformer.

Technology Transfer: IBM is offering its design services and processing capabilities to DoD contractors on a foundry basis for 1.0 micron and 0.5 micron bulk CMOS manufacturing. The fabricated parts would be radiation hardened at no additional cost or increase in complexity, and quality assurance would be maintained at the appropriate military levels.

The foundry services are being offered at several optional entry levels from customer design entry to the manufacturing foundry or use of the IBM services for design to customer requirements. The technology used would be a master image design at both 1.0 and 0.5 micron and a gate array design at 1.0 micron.

BEAMFORMER MCP

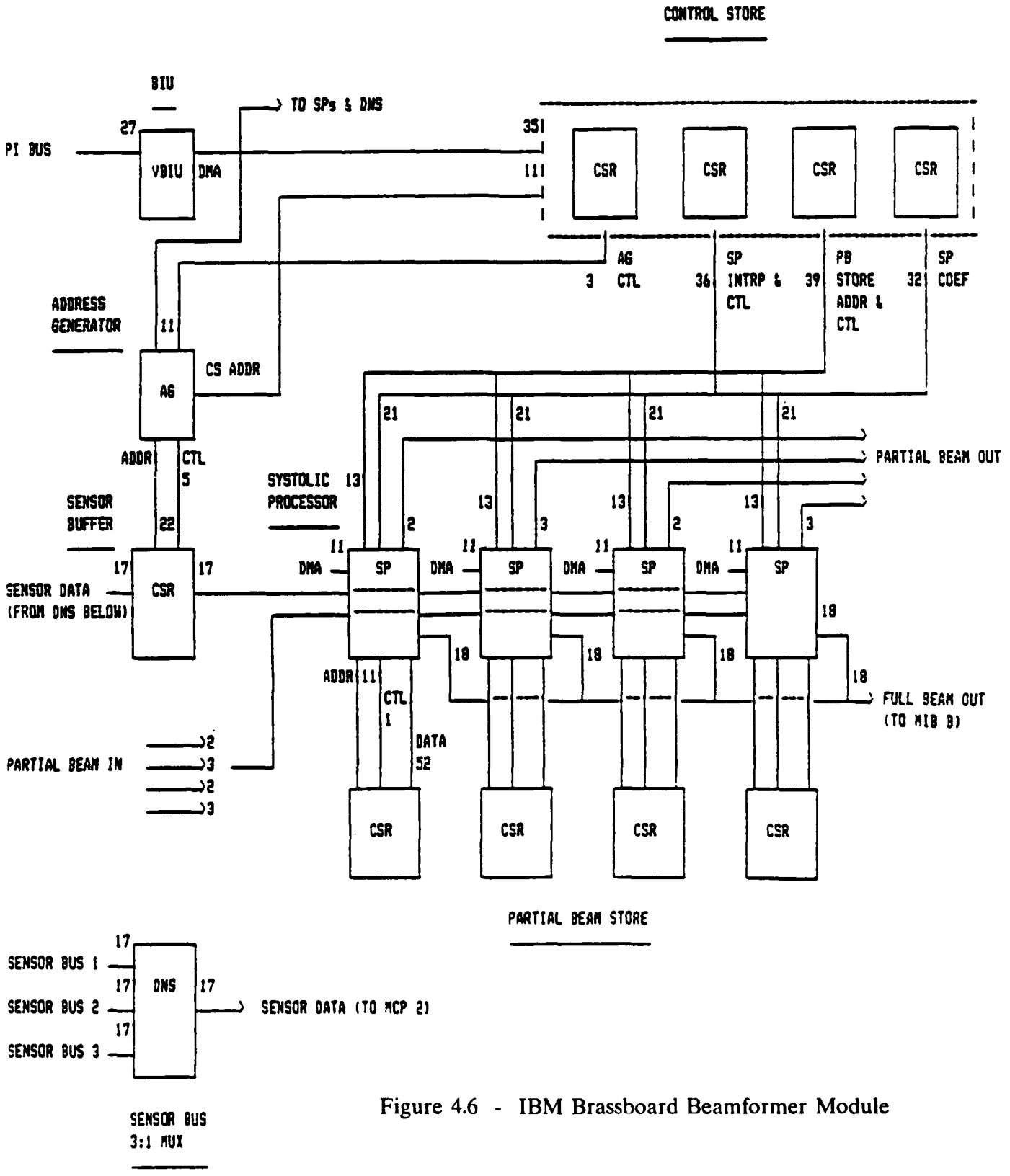


Figure 4.6 - IBM Brassboard Beamformer Module

4.4 TRW

The TRW/Motorola team is developing a unique design and fabrication methodology capable of producing "superchips" whose area, number of transistors, and functionality is up to two orders of magnitude greater than current state-of-the-art integrated circuits. To accomplish this, functional blocks called "macrocells", equal to or greater in complexity and size than VHSIC-1 chips, are fabricated on a silicon substrate and interconnected directly on the wafer to form a superchip.

A variety of technical challenges must be overcome in order to make the superchip approach viable:

- The yield of macrocell circuits on the wafer must provide a sufficient number of working circuits to assemble a fully functioning superchip.
- Spare macrocells must be included in the initial design.
- The interconnections between macrocells must be redundant to assure reliable data transfer.
- The superchip must include a built-in capability to test each macrocell for functionality and then configure the good macrocells into a single functioning superchip.

A full-blown superchip with these characteristics requires the design and verification of a large number of different macrocell types. It contains up to thirty million transistors and has built-in test circuits which automatically check the functionality of all macrocells on power-up and reconfigure them into a functioning superchip. The reconfigurability feature not only improves the probability of yielding a functioning superchip initially but also extends the life of the superchip because, as individual macrocells fail, the built-in test can automatically detect and replace the failed cells with functioning "spares". Triply redundant busses are used on the chip to ensure reliable connections between the various macrocells and I/O ports.

During 1988, the following major accomplishments occurred:

- Eight of the eleven macrocells needed to complete the demonstration superchip and the brassboard module were fabricated with optical lithography at 0.8 micron and verified as functional. The remaining three have been fabricated and are under test.

- The CPUAX superchip detailed design was successfully checked by simulation and physical layout was completed in preparation for fabrication at 0.5 micron during the first half of 1989.

Motorola Processing Technology: The initial superchip fabrication capability is being developed by Motorola at its APRDL facility in Austin, Texas. The processing is based on CMOS device technology, all optical lithography, and three levels of metalization. The lithography is accomplished with a Nikon G-line stepper machine with a high numerical aperture lens. It is expected that an I-line (shorter wavelength) stepper will be available for use in the latter half of 1989. By the end of 1988, the fabrication of macrocells at 0.8 micron was being achieved within 56 working days on a regular basis and considerably less on a "hot lot" basis.

The Motorola process has been used to fabricate successfully, at 0.8 micron minimum feature size, eight of the eleven macrocells needed for the CPUAX superchip and for the other chips on the Phase 2 brassboard module. The CPUAX layout for 0.5 micron fabrication has been partitioned into nine sectors of approximately equal area and a separate mask will be made for each of the nine areas -- resulting in a total of over 140 masks which must be used to fabricate the superchip with all optical patterning. The macrocells which are not required for the CPUAX will be fabricated only at 0.8 micron and separately packaged for mounting on the module circuit board.

TRW Processing Technology: TRW is developing, in parallel with the Motorola effort, a 0.5 micron fabrication process based on a very similar CMOS device technology but using an Hitachi e-beam machine for the critical dimension levels and optical lithography for the non-critical levels. A full flow 0.5 micron process is near completion and is being checked by fabrication of an AG macrocell at full 0.5 micron design rules along with a special test chip. The e-beam/optical process flow will be fully validated and then used to fabricate a CPUAX.

Design: The CPUAX superchip is the "computing engine" of the TRW Phase 2 brassboard module. Eight different macrocell types are required for this chip. All of these have been designed at 0.5 micron. However, the macrocells are all being first fabricated at 0.8 micron in order to verify functionality before proceeding with the 0.5 micron fabrication of the CPUAX. Five of them have been verified in silicon at 0.8 micron as fully functional. The microcontrol macrocell has a minor design discrepancy which can be by-passed (for demonstration purposes) through appropriate software changes. The fabrication at 0.5 micron will involve no changes in the design of the macrocells, merely a new set of masks using the same design database. A list of the macrocells, their characteristics, and their status for 0.8 micron fabrication are shown in the table on the next page.

An operating CPUAX requires 64 active macrocells out of approximately 150 available on the chip. These active macrocells contain approximately 1.7 million active transistors (out of 4.1 million available on the chip). Physically, the chip measures approximately 1.5 inches x 1.6 inch, has 275 I/O ports, and dissipates 17.4 watts. It is designed to perform 200 million floating point operations per second.

TRW VHSIC Chip/Macrocell Characteristics *

Name	Size (mils)	Devices	Power (W)	I/O	Test %	Fab (0.8 micron)	Functional
Multiply/Accumulator	219x330	39K	0.97	113	99.8	Done	X
Address Generator	195x198	15K	0.54	72	99.0	Done	X
Universal Processor	333x390	36K	1.0	118	95.8	Done	X
Microcontrol Unit	258x321	24K	0.7	104	99.5	Done	X **
Bus Interface Unit	210x243	35K	0.03	117	95.6	Done	
Memory Write Interface	126x188	15K	0.28	110	99.9	Done	X
Memory Read Interface	117x158	14K	0.28	74	99.8	Done	X
Arithmetic Logic Unit	240x393	40K	1.0	116	99.5	Done	
1K Programmable RAM	84x87	30K	0.02	20	-	Done	X
Storage Element	75x339	37K	0.49	188	-	Done	
Column Disable Block	92x116	5K	0.59	100	-	Done	X
CPUAX	1500x1600	4.1M	14.0	275	-	07/89	

* All macrocell dimensions are shown for 0.8 fabrication. The CPUAX superchip will be fabricated only at 0.5 micron at the dimensions shown. After self-test and configuration, 1.7 million of the transistors in the CPUAX will be active.

** One bit missing on some registers but can be operated as-is for demonstration.

Brassboard Application: The brassboard module is designed to demonstrate the computational power and operational flexibility of the superchip concept. A schematic diagram of the module architecture is shown in Figure 4.7. Two modules are being designed. The first will be populated with 0.8 micron macrocells in single chip packages (SCPs) and then interconnected on the circuit board into the CPUAX configuration and the control functions. The interconnections between the SCPs forming the CPUAX function limit the operation of this module to a 25 MHz clock rate. The second version will contain the single 0.5 micron CPUAX superchip plus the peripheral control functions using 0.8 micron chips as before. It will be mechanically interchangeable with the first version. Although this CPUAX is able to support a 100 MHz clock speed in a full superchip environment, the brassboard I/Os will only allow a 25 MHz clock and, therefore, only a 50 MFLOP throughput can be demonstrated. The mechanical and thermal designs of the module have been completed and a prototype package for the CPUAX is being fabricated.

Interim technical reports for the TRW Phase 2 contract are listed as references 4.15 through 4.21.

VHSIC | TRW MOTOROLA

Demonstration Module Features

- Demonstrates the functionality of the CPUAX SuperChip (FFT), Universal Processor (BIST) and Bus Interface Unit (PI-bus & TM-bus)
- Shows the 3 chip types operating in one integrated system
- Macrocell based CPUAX board emulates SuperChip operation

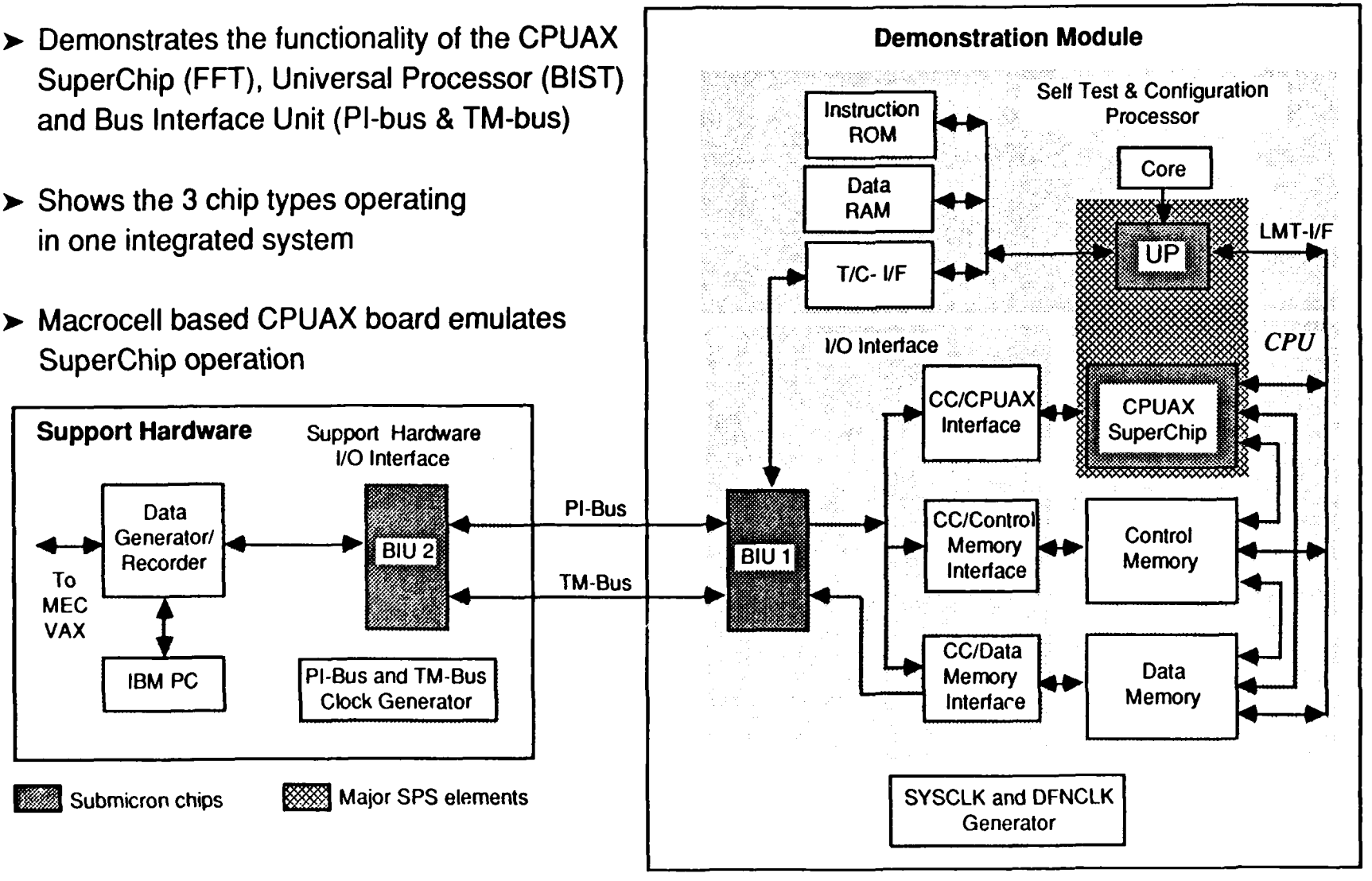


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Figure 4.7 - TRW Brassboard Demonstration Module

CHAPTER 5

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CHAPTER 5 - PHASE 3 AND OTHER SUPPORTING TECHNOLOGIES

VHSIC Phase 3 is comprised of a group of tasks to develop various technologies needed to support the main objectives of the VHSIC program. In contrast to Phases 1 and 2, which are large, comprehensive, multi-technology programs, the Phase 3 projects are more sharply focused on the areas of key technologies, equipment, and design tools needed to transform VHSIC technology into a readily usable industrial capability. Many of the original contracts ran concurrently with Phase 1 and have been completed. Others have begun more recently and are continuing during the Phase 2 period.

During the course of these supporting technology developments, some items were released from the Intenational Traffic in Arms Regulations (ITAR). These include the VHSIC Hardware Control Language (VHDL), interoperability standards, the Tester Independent Software Support System (TISSS), packaging, and the Architectural Design and Assessment System (ADAS). See references 5.1 through 5.5.

The status of the current projects is described below. Appendix D contains a list of the projects in Phase 3, the contractors, and points of contact.

5.1 DESIGN TOOLS / IDAS

The design automation portion of VHSIC technology is currently being developed under the Integrated Design Automation System (IDAS) program which grew out of a 1980 Phase 3 investigation of some design tools. The most notable of these were the Architectural Design and Analysis System by the Research Triangle Institute and a study of hardware description language requirements by Sperry.

The formal IDAS program began in late 1980 with plans for developing a VHSIC hardware description language (VHDL) and other tools for the efficient design, documentation, and management of VHSIC hardware and software. Another objective was to automate the design process at the system level and make it possible to assess the effects of various hardware/software tradeoffs very early in the design process. The designs could then be more responsive to system requirements.

The tools must not only be individually capable of handling designs of VHSIC complexity, but they must also be integrated into a smoothly working ensemble. This latter goal is achieved by requiring that all tools be capable of accepting designs expressed in the VHDL. If a tool operates at the algorithmic level, then, where feasible, the algorithms should be expressible in Ada as a common high order language. The use of these tools is being especially promoted at Service in-house design centers.

The IDAS program is organized into the four major task areas described below. The contractors currently active in the development of IDAS are listed in Appendix D.

5.1.1 VHSIC Hardware Description Language (VHDL)

The DoD faces the need to procure and maintain systems over a twenty year or more life cycle. Decisions made at the initial design phase have a major impact on the costs during the procurement and logistics processes. Control has been very difficult and expensive in the past because of the many different record keeping systems into which the processes of acquisition and maintenance have been fragmented. Even with automated systems, the flow of design information between different steps in the process has been hindered by the lack of design representation standards. The VHDL program was initiated in order to establish a common DoD language with which all the elements of the design, acquisition, and logistics processes may communicate. The first step to address these problems was the design, implementation, and validation of a minimum suite of VHDL support tools (analyzer, simulator, and design library). The next step undertaken by the VHSIC program was to promote the interface between VHDL and a number of automation tools. Finally, to accelerate the system design and validation process, the VHSIC program undertook several research and development projects oriented at advanced system design automation.

5.1.1.1 VHDL Language Definition and Development

The definition and development of VHDL is the cornerstone of the IDAS program, and is being carried out under a contract with Intermetrics, Inc. Implementation of software started in August 1984, and has continued into 1988. The software tool set developed included an analyzer, design library manager (DLM), reverse analyzer, and simulator. In September 1987, a VHDL language version for IEEE standardization was released, and, on December 10, 1987, the VHDL was approved as IEEE Standard 1076. Adoption of VHDL as an IEEE standard was a major VHSIC milestone, a step that ensures that VHSIC designs documented in the VHDL will be readily transportable throughout the commercial and military IC design communities. The VHDL IEEE 1076 software (analyzer, design library manager, and fully interactive simulator) was delivered during 1988. Software is now production quality and resident on VAX/VMS and Berkeley UNIX on Sun workstations. A UNIX version for the VAX is scheduled for delivery in April, 1989.

A VHDL newsletter is available from Intermetrics which regularly publishes information related to VHDL.

5.1.1.2 VHDL Independent Validation and Verification (IV&V)

The purpose of the IV&V effort was to test the VHDL software in actual use in the field. The primary contract for this effort was awarded to the United Technologies Microelectronics Center (UTMC) in August 1985. The work was divided

into two parts. The contractor performed an initial test of the VHDL software and then acted as a focal point for secondary testing at "beta" sites. User comments from the beta test sites have been incorporated into the IEEE 1076 version of the VHDL software. The contract was completed during 1988 and this part of the program concluded successfully with VHDL as a production tool.

5.1.1.3 Joint U. S. / Canadian IBM Rehost

Under the Joint US/Canadian program started in July 1987, the VHDL tools are being adapted for use with IBM mainframes. The U. S. is providing the VHDL software, graphics interface, EDIF interface, validation tests, and technical consultation. The Canadian contractor, Bell Northern Research (BNR), will install the VHDL software on the IBM machines and integrate some of its own design tools into that VHDL environment. A plan for the rehost has been developed, and rehost work started November 1988 and should be complete by April 1989. The BNR tool development and integration is to continue through 1991.

5.1.2 VHDL Technology Insertion

The goal of the VHDL Technology Insertion program is to provide advanced design tools to support the designer using the VHDL. Beginning in August 1985, the VHDL program has awarded eight contracts. Those current in 1988 are listed in Appendix D.

5.1.2.1 Workstations/Interfaces (Vista)

The purpose of this effort is to develop terminals with interfaces which assist the designer using VHDL.

Gould (via subcontractor Vista Technologies) has developed a prototype generic workstation interface for VHDL using a SUN 3 workstation, which will automate the generation of VHDL code and check for internal consistency. The work has progressed successfully with the final software delivered in December 1987 to the Army at Ft. Monmouth and the Navy at the Naval Research Laboratory for evaluation. The new VHDL workbench allows a designer to input schematic diagrams and have VHDL structural descriptions compiled in real time. If functional descriptions are desired, the system provides "hand holding" by means of a syntax directed editor. The user can create VHDL code even with limited knowledge of the language. This system should become the designer's entry into the world of VHDL. The technology embodied in this program is being commercialized by Vista Technologies, and Vista is under subcontract to Intermetrics on the Canadian Rehost contract (Section 5.1.1.3) to provide a graphics interface to the Intermetrics tool set.

5.1.2.2 Integration of VHDL and ADAS (Research Triangle Institute)

The goal of this contract was to integrate RTI's Architectural Design and Assessment System (ADAS) with VHDL in such a way that system designs may be captured (hierarchically) with ADAS and archived in VHDL and to enhance the ADAS tool set. To support this effort, extensive modifications to the ADAS graph editor, data base, and simulator were carried out. The net result is an integrated design system which takes advantage of the modeling and simulation capabilities of both ADAS and VHDL. Using these tools, designers can capture and simulate their designs at several levels of abstraction.

During 1988, implementation of the modifications to ADAS to support the VHDL interface was completed. The original interface was built around VHDL Version 7.2. After VHDL was standardized by the IEEE in December 1987, the interface was modified to support the new VHDL standard.

The ADAS simulator was also extensively modified under this contract. The modifications reduce the need to use functional simulation to model complex systems. The contract was completed in September 1988, and the results of the contract work were delivered to the Government. See references 5.6 and 5.7.

5.1.2.3 Synthesis Tools (Honeywell, JRS Research, and Unisys)

The purpose of these efforts is to derive chip design data automatically from a VHDL behavioral description.

Honeywell has developed a tool called V-Synth which determines a useful chip architecture from input that is algorithmic in nature and contains an implied structure. The output is an architectural description of a microprogrammed device in VHDL and the microcode to drive the device. Honeywell delivered a prototype of the software in June 1987 and the final version in November 1987. In 1988 Honeywell upgraded the VHDL Synthesis System under the VHSIC Phase 2 contract to be compatible with the IEEE Standard VHDL. The register transfer level VHDL behavioral description of the Phase 2 BIU chip design was synthesized using V-Synth. The generated microcode required 31 words of 40 bits each. The size and expected performance of the design were being evaluated.

JRS Research has developed an Automated VHDL/Microcode Compiler Synthesis and Design System (AMSDS) which synthesizes a microprogrammed processor architecture from an Ada program and a VHDL description of chips. Output from the program is a VHDL description of the processor and optimized microcode for the processor. Further details are given in Section 5.1.3.2.

5.1.2.4 Silicon Compiler Interfaces (Research Triangle Institute)

RTI, Silicon Compiler Systems, Inc., and E-Systems completed the development and demonstration of the VHSIC Silicon Compiler (VSC). This effort involved the integration of ADAS, Genesil and VHDL. Using the VSC, engineers can capture and model designs from the system to the transistor level. Designers can then use Genesil as a fabrication mechanism for new integrated circuits identified during the design process. Information is transmitted among the tools in the VSC with special purpose interfaces which provide the desired capabilities. Major capabilities include:

- The representation of Genesil objects in ADAS such that designers can evaluate the performance and functionality of a proposed chip design in the context of the overall system,

- The ability to partition a hardware hierarchy based on its estimated area and power dissipation, and

- The generation of VHDL functional models from Genesil which can be incorporated into the hierarchical VHDL models produced by ADAS.

As part of the contract, E-Systems used the VSC tools to develop and simulate an image processing system. Part of the system included the development of a special purpose ASIC which performed the core calculations required for the imaging application. The simulation was done in VHDL Version 7.2.

The initial version of the VSC used VHDL Version 7.2. After the IEEE standardized VHDL, the VSC tools were converted to the 1076 standard. The contract was completed in September 1988 and the results were delivered to the Government.

The CMOS interface effort by National Semiconductor complements this by making it possible to produce the chip designed with the Genesil compiler on the National Semiconductor CMOS VHSIC pilot line. This provides an experimental demonstration that the hardware output corresponds with the input design specifications. See references 5.8 through 5.13.

5.1.2.5 VHDL Models

As part of its effort in the development of systems design tools reported in Section 5.1.3.2, JRS improved the comprehensiveness of the VHDL modeling done to include complex behavioral models, detailed physical attributes, and a greater variety of devices. JRS produced, analyzed, and simulated VHDL 1076 models of the TRW, TI, and Honeywell Phase 1 VHSIC chips.

5.1.3 System Design Tools

Under this program advanced design tools are being developed which aim at making the higher (system) level of the design process more automated and more efficient. The efforts in this area will provide a variety of tools in fields such as design verification, design for test, advanced system synthesis, and life cycle cost modeling. Several contracts have been awarded to universities in order to develop advanced concepts in this subject area and, at the same time, introduce VHDL into the academic community. Work on this part of the program began in September 1986. All contracts should be completed by December 1989.

5.1.3.1 VHDL Annotation Language (VAL) (Stanford)

VHDL Annotation Language (VAL) is a language extension of the VHDL which allows designs to be specified as annotations to VHDL. Hardware behavior is defined by simple abstract specifications and the behavior is related to more detailed architectural descriptions in VHDL. VAL augments VHDL by supporting powerful constructs for timing and abstraction, and simpler constructs for parallelism. It also provides some basic constructs for expressing correspondence between VAL specifications and VHDL architectures. VAL annotations are used to check consistency between VAL specifications and VHDL architectures during simulation.

During 1988, the design of VAL was completed. A VAL transformer is being implemented which translates VHDL descriptions with VAL annotations into proper, self-checking VHDL source code. The VHDL source code is compiled and simulated by standard VHDL tools. Any inconsistency between the original VAL specification and VHDL architecture is detected and automatically reported during VHDL simulation. The transformer was demonstrated at the Design Automation Conference in June, 1988, and at the VHDL Users Conference in October, 1988. The VAL transformer will be available during the 2nd quarter of 1989. See references 5.14 and 5.15.

5.1.3.2 AMSDS - Automated VHDL Microcode Computer Synthesis and Design System (JRS Research Laboratories)

The project goals are to provide an integrated set of high level design automation/CAD tools for hardware/software design of high performance embedded computers for DoD applications. Included in the tool set are (1) an Ada to microcode compilation system that is automatically retargetable from VHDL, (2) an automated system that synthesizes designs described in VHDL from specifications written in Ada, and (3) links to external tools including silicon compilers.

Background: JRS has been actively pursuing the development of this technology for the past nine years, including its association with the VHSIC Program since 1984. Versions of Ada to microcode compilers for four VHSIC Phase 1 processors were developed along with VHDL models of the chips. A functional prototype of the AMSDS was delivered to the VHSIC program offices of the three Services in June 1987.

1988 Highlights: During 1988, the following major achievements were made:

- o Extended the synthesis tools to include an automated hardware/software tradeoff engine and an architecture selection capability based on expert derived rule sets.

- o Extended the capability of the microcode compilation system by adding more sophisticated optimization in the allocation of resources, scheduling/compaction, and machine dependency.

- o Successfully integrated with the Concorde Silicon Compiler system from Seattle Silicon, Inc. and demonstrated the ability to automatically process specifications (in the form of Ada programs) to silicon (in the form of control tapes for foundry fabrication).

- o Integrated the AMSDS tools with an object oriented DBMS and a sophisticated process control system to provide a framework for integrating a variety of CAD/CAE/CASE tools.

- o Delivered prototype software of the synthesis system in August 1988. Final delivery is scheduled for March 1989.

See references 5.16 and 5.17.

5.1.3.3 System Level Tools for the Advanced Design AutoMation (ADAM) System (University of Southern California)

Prototype design tools are being developed to allow a designer to specify requirements for a design in VHDL and produce a register transfer level description. A user interface is designed to provide the capability of entering design information into ADAM by writing descriptions in either VHDL or a natural language (i.e. English-like). A synthesis subsystem takes a behavioral specification of the design and creates a register transfer level data path and a schedule of operations to be performed so that the data flow can be pipelined. An object oriented database manages the

information for the system.

During 1988, the natural vocabulary of the language interface for entering system specifications was greatly expanded. New concepts and patterns have been added to allow the designer to talk about conditional events and iterations of events, that is, loops. Specifications for the mapping of each VHDL construct to each internal data structure construct in the ADAM system have been written.

The complete synthesis subsystem is operational. The designer can enter a specification of design behavior at the abstract level and a register transfer datapath can be produced along with a pipelined schedule. The software has been tested for a number of small but relevant examples.

The commercial relational database (SUN Unify) has been personalized to contain digital design data, and a user interface called EVE has been completed. EVE allows the synthesis programs to access the design data as objects rather than the tables and relations which are actually stored in the database. Example queries have been used to test the database.

A utility program has been written to provide the database with design specifications so that the synthesis programs can be tested with the EVE database interface. The area estimation programs which form part of tne integrated system have been specified and several of the packages completed. Packages for estimating functional area, routing area, control area, and register and multiplexer area have all been written, tested, and verified. Documentation for the user interfaces to the database has been written and provided to programmers of the synthesis software for use in system integration. See references 5.18 through 5.24.

5.1.3.4 Hierarchical Design for Testability (Research Triangle Institute)

Utilization of the Test Engineer's Assistant (TEA) system methodology and computer-aided design (CAD) tools enables design and test of digital hardware to occur in parallel with system functional design and results in systems that are maintainable at a lower life cycle cost. TEA provides a methodology and a supporting CAD system that allows the system designer to meet testability requirements. This is accomplished by supporting design for testability and built-in test (BIT) techniques at all levels of design abstraction. TEA interfaces directly to ADAS tools and through ADAS to VHDL.

RTI developed five tools in 1988. The Design for Testability Guideline Checker identifies untestable structures and recommends alternatives that are more testable. BIT Recommendation divides a board into ambiguity groups (AGs) for fault isolation testing and recommends a class of BIT techniques for each AG. BIT Overhead Summary calculates the approximate hardware overhead (i.e., test points, BIT support modules, and additional I/O) associated with the implementation of a particular board level BIT technique. BIT Placement Recommendation generates a new schematic of

the board with a sample implementation of the given technique. System Summary itemizes the incremental hardware overhead attributable to added testability. The contract was completed in December 1988. See references 5.25 through 5.30.

5.1.3.5 Analog Design with VHDL (Dartmouth University)

This effort explored the use of the VHDL linkage port to escape to other styles of design. An object oriented system based on Prolog was constructed, and rules to allow the design of different filter types were generated. The contract will be completed in 1989.

5.1.3.6 Object Oriented Chip Design Using VHDL (Rensselaer Polytechnic Institute)

An advanced design tool is being developed that uses a novel way of producing a design. The designer will have available a set of "components", or building blocks, in a library from which he can build a chip. These blocks will be keyed like jigsaw puzzle pieces so that the design process will be analogous to putting a jigsaw puzzle together. As the design progresses, the VHDL description and the chip physical layout will be produced automatically. The system is now under construction and scheduled for delivery in September 1989.

5.1.3.7 Artificial Intelligence for VHSIC Systems Design (AIVD) (Research Triangle Institute)

An advanced design tool is being developed that uses a novel way of producing a design by working at the systems level. The designer will have available a set of "components", or building blocks from which he can build a chip, or in the general case, an electronic system. The user will interact with the system through an object oriented interface which will permit access to components in an object oriented data base (the ROSE database developed at RPI). The system will consist of an editor, the design library, a search engine and a tool for insertion and extraction of designs expressed in VHDL. As the design progresses, the VHDL description will be produced automatically.

During 1988, the high level specification phase was completed. The system architecture and the implementation strategy were defined and the system is scheduled for delivery in September 1989. See references 5.31 and 5.32.

5.1.4 Engineering Information System (EIS)

Any design automation system requires a framework within which hardware and software information can be managed from the inception of a design through its complete life cycle. The EIS will allow data to reside in a heterogenous hardware environment but present a homogenous view of those data to the designer. The DoD is working with industry and the IEEE to obtain a common standard. A joint DoD/IEEE workshop was held at the University of Arizona in January 1986 to generate EIS requirements.

The EIS contract was awarded in July 1987 to Honeywell as the prime contractor and a team comprised of Computer Corporation of America, TRW, CAD Language Systems Inc., McDonnell Douglas Aerospace, and Arizona State University.

The preliminary design review was held on November 13-15, 1987. Thus far, the following has been accomplished: the system requirements were refined; the top-level system design has been completed; the design of the user interface management system, the user interface development guidelines, and the specifications for portability services interfaces have been completed. The specification for the object management system is nearing completion, and draft models for electronic design information and administrative information have been completed.

In order to enlist the cooperation of industry, so vital to the success of this effort, Honeywell has participated in 28 conferences and workshops and 16 standards group meetings. A monthly information newsletter is published. A major industry workshop was held on November 14-18, 1988. A critical design review is scheduled for June or July 1989.

5.2 LITHOGRAPHY

5.2.1 E-Beam Lithography - Hughes / Perkin Elmer

E-beam lithography equipment with a capacity for high wafer throughput was developed to support the fabrication of 0.5 micron feature size VHSIC chips on a pilot line basis. Perkin Elmer Corporation (PE) developed such a machine (the AEBLE-150) under a VHSIC contract which started in 1981 and finished with final acceptance test by the Army in February, 1985. PE undertook an additional, independent, three year effort to improve the resolution and overlay accuracy in order to meet the full machine specifications. An AEBLE 150 meeting the requirements was accepted by Motorola in September 1988. This successful development provides a capability for e-beam patterning which meets the needs of the U.S. for a machine capable of moderate production of submicron chips. Further improvement of the capabilities of this machine to 0.25 micron resolution is being undertaken in a two year contract with the DARPA MIMIC program office.

5.2.2 X-Ray Lithography - Perkin Elmer

The goal of this program is to develop an X-ray lithographic machine capable of patterning submicron chips at high throughput under moderate production volume. The key features of the X-ray step and repeat (XSAR) machine specifications are:

- o 0.5 micron resolution
- o 20 wafer levels per hour throughput (with a 10 microJoule/cm^2 resist sensitivity) and four inch diameter wafers
- o development of a source for the fabrication of high quality masks
- o installation and testing of the tool in a VHSIC Phase 2 pilot line

At the beginning of 1988, the first machine (XSAR-1) was fully operational and had demonstrated 0.5 micron resolution, 0.1 micron overlay accuracy, and line width control of 0.06 micron.

During 1988, Honeywell was selected to install and evaluate the machine in a pilot line environment. Two chips have been designated as the devices to be fabricated for demonstration of the machine's capabilities. Masks were fabricated for these devices, test exposures were made on the XSAR-1 at Perkin Elmer, and the Army began acceptance tests on the machine. A second machine (XSAR-2) has been assembled for installation at Honeywell and lithography tests on that machine have begun. Testing of new X-ray resists from Spire (see next project write-up below) was started and preliminary results are encouraging.

A demonstration of the XSAR-1 machine is scheduled for January 1989 to be followed by installation of XSAR-2 at Honeywell for extended evaluation.

5.2.3 X-Ray Lithography - Spire Corporation

The goals of this program, begun in February 1988, are (1) to develop a simple, low cost, X-ray exposure station for X-ray resist and mask testing, (2) to develop high sensitivity, high resolution resists for X-ray lithography, (3) to test these resists in a pilot line environment, and (4) to provide a domestic, commercial source for these resists.

During 1988, the first exposure system was built, and new resists provided by the subcontractors were tested. A second exposure station is being assembled and will be installed at a subcontractor's laboratory in 1989. Masks for the X-ray exposure testing have been fabricated and delivered. Subcontractors are Rohm and Haas, Mead Technologies, and Perkin Elmer.

5.2.4 Laser Pantography - Lawrence Livermore National Laboratory (LLNL)

The goals of the LLNL Laser Pantography (LP) Project are to:

- o Develop a means for implementing robust, compact, lightweight, high performance digital electronics systems immediately suitable for military applications.
- o Develop an affordable, end-to-end technology that enables the rapid synthesis of prototype digital electronic devices and systems
- o Create a manufacturing capability that is highly flexible and thus can keep pace with the rapidly evolving needs of DoD for advanced digital electronics systems.

To attain these basic objectives, research has been pursued with the technical objective of developing a vertically integrated, computer-automated capability for producing high performance digital systems in hybrid wafer-scale integrated (HWSI) circuit format. For instance, a VHSIC (1.25 micron) double level metal interconnect capability has been established to provide rapid turn around of VHSIC class gate arrays for HWSI. The technology for fabrication of high performance silicon printed circuit boards connecting such gate arrays and other high performance VHSIC on a single silicon wafer has also been demonstrated, including low loss signal propagation at 0.75c (23 cm/ns) between the IC components across the wafer. To remove heat from such systems-in-silicon, the performance of microchannel heat sinks has been significantly enhanced: A 1-cm^2 resistive heated area of silicon wafer has been operated at 2900 watts, more than twice the previous record. Active devices such as laser diodes and rf power transistors have been attached to microchannel heat sinks and operated at high average power levels. In the case of laser diode linear single bar arrays, a heat removal capability of 110 W/cm^2 with a 10°C temperature rise has been achieved. See reference 5.33.

Multichip modules using hybrid wafer-scale integration technology and VHSIC memory chips from National Semiconductor have been delivered to an LP Project industrial partner, Fairchild Space Company. Four 10-chip radiation hard memory hybrids were shipped, on schedule, in May 1988. These parts were fully tested to pertinent Mil-Spec 883C Class B methods, including all hermeticity, temperature, and mechanical tests.

The ten-chip VHSIC memory hybrids are currently undergoing system integration at Fairchild Space Company. They will be incorporated into a Solid-State Recorder that will undergo system environmental and mechanical testing. The Solid-State Recorder will fly on the Air Force P87-2 spacecraft currently planned for consortium launching in the third quarter of FY 1989.

5.2.5 Advanced Wafer Imaging System (AWIS) - GCA Corporation

The VHSIC program office supported the development of this advanced optical

lithography machine by GCA in order to provide a capability for high throughput wafer patterning in a production environment. The AWIS was installed at IBM, Manassas, VA, late in 1987. It was fully tested and accepted in March 1988 and then evaluated under operational use. The tool has met all specifications except uniformity of the pattern over the wafer. This was attributed to a slight tilting of the lens which can be corrected by adjusting the lens position. Optical lithography with 0.35 to 0.5 micron resolution has been consistently demonstrated. This tool provides an important potential capability for the high resolution, high throughput, lithography at low cost per wafer which will be needed for both commercial and military IC manufacturing during the next decade.

IBM has provided access to the machine for industry, university, and Government personnel to conduct experiments in deep ultraviolet lithography at 248 nanometers (the wavelength of the AWIS illuminator). These experiments have been of great value in evaluating several resists being developed by at least ten companies. More than ten papers were published through the use of this advanced lithography tool.

5.3 RADIATION HARDENING

5.3.1 VHSIC Radiation Hardening Program

The objective of the program is to harden the VHSIC technologies to meet the DoD space and missile radiation survivability requirements. Reports of earlier work in this program are given in references 5.34 through 5.39. Work during 1988 is reported in references 5.40 and 5.41 and in the following paragraphs.

(a) General Electric/RCA - CMOS/SOS

GE/RCA has successfully transferred its radiation hardened process from Somerville, NJ to its Microelectronics Center (MEC) at Research Triangle Park, NC under a DNA contract funded by VHSIC. Fully functional VHSIC/DNA 8K x 8 static rams have been fabricated and will be undergoing extensive testing in 1Q89. Initial results verify that the dose rate upset level is greater than 10^{10} rad(Si). Improvements will be made under the SDI funded SAT 8.1 program.

(b) Westinghouse/National Semiconductor - CMOS

With VHSIC funding, DNA has contracted Westinghouse to radiation harden the VHSIC bulk CMOS process at National Semiconductor (NSC) and at Westinghouse (WEC) (Baltimore). Recent results show that Westinghouse has achieved space radiation hardness with the VHSIC 10K gate array fabricated in Baltimore. These hardened arrays will be made available through the Chesapeake Group, with WEC and NSC both capable of fabricating the radiation hardened arrays. National Semiconductor has demonstrated on their VHSIC line the feasibility of producing space hardened 64K static RAMs operating at 3.3 V. Work is

continuing to achieve space hardness including single event upset immunity in 5 V VHSIC 64K SRAMs by 2Q89. The major problem continues to be radiation induced increases in standby leakage currents.

(c) Hughes Aircraft Corporation - CMOS/SOS

The Hughes Aircraft Corporation VHSIC Phase 1 CMOS/SOS technology now available is radiation hard to space levels. Further improvements in radiation hardness are being made under the SDI SAT 8.1 program.

(d) Texas Instruments, Honeywell, and TRW - Bipolar

During 1988, investigations to harden bipolar against radiation induced latchup were completed. No single event upset (SEU) hardening has been done for the bipolar technologies, but SEU hardening techniques have been demonstrated under a separate DNA sponsored program. The VHSIC bipolar technologies are available and should be considered for space and missile applications.

(e) IBM - CMOS Submicron

IBM has produced fully functional submicron chips. Initial radiation test results indicate that the 0.5 micron chips meet space radiation requirements. Further process enhancements are being investigated. Complete radiation evaluation should be completed by May 1989. Space radiation hardened submicron technology should be available at IBM in late CY89. The availability of this advanced IC technology will be a major breakthrough for the users of radiation hardened microelectronics.

5.4 QUALIFICATION, RELIABILITY, AND TEST

5.4.1 TISSS (Tester Independent Software Support System)

TISSS is a system for the automated generation and maintenance of electrical test specifications and test programs for VHSIC devices. The system includes a database-centered software support system that is independent of both the CAD (computer aided design) and test environments. The capability provided by TISSS will enable the user to develop and maintain high reliability specifications in a standardized, transportable, and computer-accessible format and to automatically generate test programs. The Government use of TISSS will significantly reduce the time required to insert advanced technology microelectronics into operational systems. In addition, the device data stored in the TISSS database can be used for reprocurement of devices no longer being manufactured.

Full scale development of the TISSS was begun by Harris Corporation in September 1985. TISSS documentation software is currently available for review, and TISSS software is

available for beta site use. Beta site use of the TISSS began at IBM and Honeywell for testing the GVSC (Generic VHSIC Spaceborne Computer) devices that are currently under development.

TISSS training was held for Government personnel, and additional training is planned for the GVSC TISSS beta sites. TISSS training is also available to all other beta sites on video tape. An on-line TISSS training program also accompanies all beta site releases of the TISSS.

Insertion planning for the TISSS will be based on beta site use at IBM and Honeywell, who are tasked to develop operational procedures and guidelines for TISSS use. DoD has recommended the establishment of an operational TISSS at DESC.

The TISSS Vector Language (TVL) is currently undergoing IEEE standardization to permit better acceptance of its use for supply of all test vectors to DoD for devices developed. A Data Item Description (DID) for TVL will be available for use in 1989, and the TVL will be introduced for incorporation to MIL-STD-454 after industry comments have been incorporated from the IEEE standardization process.

The TISSS is currently under maintenance and available for use by all requesters. Manuals, specifications, and other documentation are listed as references 5.38 to 5.44. Preplanned product improvements (P^3I) have been initiated by the Government under the control of a Government Change Control Board (CCB).

Extensions of the TISSS to support the next level of electronic integration, LRMs (Line Replaceable Modules), has begun for the ATF (Advanced Tactical Fighter).

5.4.2 Qualification Procedures - QML (GE, ATT, Honeywell)

The VHSIC chips being produced for use in military systems must be qualified for military use. The current standards for JAN qualification briefly described in Section 3.2 are proving to be very costly and time consuming to implement for VHSIC class chips. More appropriate standards have been proposed in the past and are now being developed. The new standards are based on establishing qualified manufacturing lines (QML) which can produce fully qualified parts without the costly testing of each individual part. This process of "generic" qualification for military products depends on tight control of the manufacturing process in order to assure that the quality and reliability of the product, once established, remain within required limits.

The silicon microcircuit QML effort is accelerating. The DoD and the Semiconductor Industry Association are studying this new qualification strategy for use in the manufacture and procurement of semiconductor devices.

The alpha sites, AT&T and General Electric, are scheduled for certification audits. Beta site volunteers, GE Solid State, Harris Semiconductor, IBM, Intel, National Semiconductor, Texas Instruments, and VLSI Technology have started to address the certification requirements. The next draft of the proposed QML General Specification MIL-I-38535 will be released in the first quarter of 1989.

Efforts are ongoing to include linear devices and GaAs technology into the Generic Qualification concept.

5.4.3 Qualification Procedures - QML (IBM)

A 24-month modification to the Phase 2 contract was awarded on June 1, 1988 to extend the QML procedures to 0.5 micron technology. The objective is to: 1) develop and implement statistical process control (SPC) techniques; 2) design and implement process control monitors and standard evaluation circuits as in-line process monitors and reliability indicators; 3) develop a reliability prediction model; 4) validate the model through testing; and 5) certify and qualify the 0.5 micron CMOS process as a qualified manufacturer for inclusion on a qualified manufacturers list (QML).

IBM has initiated a SPC program. A team has been formed, schedule developed, training initiated, and critical process modules defined and documented. A first order reliability model has been generated. Life test data for 1.0 micron CMOS technology is being generated for verification of the model. A close working relationship has been formed with the industry/DoD Generic Qualification Working Group to assure incorporation of these results into the QML program.

5.4.4 Reliability Assessment of Gate Arrays (GTE)

The project focus is on the generic qualification of gate arrays and the reliability of representative products. The draft final report was received in December 1988 and contains the contractor's test results and suggestions for refining and updating qualification criteria of the MIL-M-38510/600 and /605 detail specifications. A set of step-stress and life-tests was done on CMOS standard evaluation circuits, and failure analysis was completed in November 1988. The tests were structured to observe electro-migration and hot electron effects. Test results will be used to modify the /605 detail specification where necessary to insure quality and reliable gate array products.

5.4.5 Non-Destructive Bond Testing (Vanzetti Systems and Sonoscan)

1. Vanzetti Systems. This effort is one of two 24 month investigations to develop a method for testing the quality of metallurgical bonds formed in the process of connecting VLSI/VHSIC chips to their packages by means of tape automated bond (TAB). This program generated a test method using laser-thermal non-destructive techniques that will be submitted for coordination and implementation in MIL-STD-883.

The effort has also developed a non-destructive evaluation technique with the necessary resolution to assess these chip and package metallurgical bond sites and has established the parameters that distinguish an acceptable bond from a defective one. The contract was awarded and effort begun in April 1986.

The recent growth of TAB technology has evoked broad industrial interest in automatic inspection methods for TAB bonds where lead widths can be as small as two mils. Under Air Force funding, the Vanzetti company has extended present inspection methods to these smaller sizes. An experimental laser/thermal inspection system for TAB bonds has been in operation

since the summer of 1986 and routinely reveals lifted and deformed leads, contamination, solder quality anomalies and other deviations from normal. The laser heating spot is just two mils in diameter. Exposure durations as short as 60 msec raise the target surface temperature by some 50-100° C above room temperature. With somewhat longer exposures, the solder can be reflowed. This phenomenon is being explored as a means of repairing lifted leads immediately after they are found during the inspection process and, indeed, as a possible method of manufacturing soldered TAB bonds in the first place. Combined with the continuous thermal monitoring which is already available, it makes possible the precise control of solder temperature, joint by joint, followed by the automatic inspection process.

This contract was completed in 1988. Technical Report RADC-TR-88-139, detailing the test method that was developed, has been published and distributed. See reference 5.50.

2. Sonoscan. This effort is the other of the two 24 month investigations to develop a method for testing the quality of metallurgical bonds formed in the process of connecting VLSI/VHSIC chips to their packages by means of tape automated bonding (TAB). The test method was developed, delivered, and documented under this program. The test method uses acoustic non-destructive techniques that will be submitted for coordination and implementation in MIL-STD-883. The contract was awarded and effort began in April 1986.

A matrix of TAB inner and outer lead devices with a built-in range of quality has been investigated. Each bond interface was documented acoustically and then pull-tested to develop a database upon which to formulate a specific test method. Preliminary data demonstrate good correlation between the degree of bonding and correlative pull tests (destructive). Optical inspection of the bonds prior to the acoustic microscopy could not detect differences in the bonds. This investigation was performed with well established acoustic microscopy techniques which have been adapted to TAB. In particular, the Scanning Laser Acoustic Microscope (SLAM) produces real-time images -- 30 fields of view per second -- at ultrasonic frequencies from 10-200 MHz. The speed of scan and the practicality of acoustic microscopy demonstrated in other non-destructive testing applications make the method potentially viable for non-destructive evaluation of TAB.

This work was completed in December 1988. A final report from the contractor is being reviewed for publication by RADC.

5.4.6 Reliability Modeling (IITRI / Honeywell)

The technical work on Contract F30602-86-C-0261 "VHSIC/VHSIC-Like Reliability Prediction Modeling" has been completed and a draft final report has been delivered. The contract was awarded to a team comprised of IIT Research Institute (IITRI) and Honeywell SSED in September 1986. The effort has resulted in the development of two models, a detailed model and a short form model, for predicting failure rates for VHSIC and near VHSIC CMOS microcircuits.

The detailed model is based on the characteristics of specific failure modes, manufacturer specific information such as defect density and wearout performance, and key application data including temperature and operating time. The short form model is a

condensed version of the detailed model and does not require manufacturer specific information but rather easily accessible information. The penalty in using the short model is its lower precision and accuracy relative to the detailed model.

The models account for both time dependent and defect-related failure mechanisms. A data base was built containing the life test, burn-in and environmental test results from a variety of manufacturers. Much of the data contained in this data base was used in the quantification of early life failure rates for various specific failure mechanisms. Therefore, in predicting defect-related early life failure rates, the detailed model will yield an industry wide representative failure rate. The use of actual defect densities, if properly measured, will result in predicted reliability values which are more precise and accurate than conventional regression type prediction models.

It was also determined in this study that it is these defect-related mechanisms that largely determine failure rate during most of a part's life. Wearout mechanisms have also been modeled which will provide an approximate end of lifetime as a function of the part's design rules and its particular application.

The model addresses three time-dependent mechanisms: electro-migration, time-dependent dielectric breakdown, and hot carrier effects. The model has factors for chip area, defect density, and/or minimum feature size so that changes in technology can readily be factored in. It has a correction factor to modify the model as VHSIC field experience becomes available and to modify the model for a particular fabrication process based on the availability of high quality life tests. The model can also utilize test pattern data from manufacturers in conjunction with the Yield Enhancement and Generic Qualification programs. There is a package factor which considers the number of package pins and includes the following package types: PIN grid arrays, chip carriers, and dual-in-line packages. It also has factors for EOS/ESD and whether or not the device is on the QPL/QML.

The detailed model has been validated with the life test data that was available on 1.0 and 1.25 micron processes from three separate manufacturing processes. The detailed model has also been provided on a disk for use on a PC computer. The models will be proposed for inclusion in MIL-HDBK-217 "Reliability Prediction of Electronic Equipment". See reference 5.51.

5.5 PACKAGING

Single chip and multichip packaging development and manufacturing programs have established the VHSIC packaging and interconnection methods for use in DoD electronics.

U.S. sources have been established for single chip and multichip packages for housing VHSIC chips and for tape used in Tape Automated Bonding (TAB) interconnection of chip to chip or chip to package. The copper/polyimide TAB tape from 3M is 70 millimeters wide, and is customized for the various VHSIC chips. Procedures for the inner lead bonding and outer lead bonding has been established and documented by Honeywell. The single chip package from General Ceramics based on the Martin Marietta design conforms to EIA JEDEC outline standards for the family of VHSIC packages. Input/output (I/O) lead counts of 124, 204 and 264 are available. The multichip packages from Interamics have I/O counts

of 196 and 308 and house 2 to 4 and 5 to 9 chips respectively. A four-chip VHSIC SRAM module has been housed in the smaller package by Texas Instruments with TAB interconnections to the thick film substrate. Reports on packaging during 1988 are listed as references 5.52 and 5.53.

5.6 INTEROPERABILTY

The VHSIC Phase 2 Statement of Work, issued in 1984, stated the following requirements for interoperability:

> "3.5.1 INTEROPERABILITY STANDARDS:
>
> Interface/Interoperability Standards shall be established by agreement among all VHSIC Phase 2 Submicron Contractors and the Government COTRs to assure that all chips developed under the VHSIC Phase 2 Submicron Program are interoperable, both electrically and physically. Standard voltage level(s) shall be established and utilized for all chips and input/output levels shall be equivalent for all chip interfaces, whether contained in a single or multi-chip package. A VHSIC half-micron Bus Interface Unit (BIU) chip shall be developed to facilitate module interoperability with a Standard Interconnect System Bus. The BIU and any other VHSIC chips developed under this Phase 2 VHSIC Submicron Program shall interface directly to a Standard System Maintenance Bus to be defined by agreement among all the VHSIC Phase 2 Submicron contractors and the Government COTRs. All these Standards shall be documented and delivered."

In accordance with the above paragraph, a Tri-Service Interoperability Committee negotiated four standards with the Phase 2 contractors, and the documents were delivered to DoD as part of the June 1988 VHSIC TECH-FAIR II held at the Johns Hopkins Applied Physics Laboratory. The standards exist as copyrighted documents to prevent the reproduction of multiple unauthorized versions, but may be copied in their entirety. They are "open" standards, and may be used by anyone. [For availability, see references 5.54 through 5.57.] They are also described in the "VHSIC Annual Report for 1987", reference 1.2. Since then, the Interoperability Committee has shifted its focus to the task of monitoring for compliance with the documents at their respective service Phase 2 contractors, testing products such as the BIUs created by the contractors, and promoting insertion efforts.

5.6.1 Standardization, Support, and Insertion

(a) The Electrical Interface Specification (Version 2.4, 21 January 1988), is designed to facilitate interoperability between all Phase 2 chips, new Phase 1 chips, and standard TTL-I/O chips. Its purpose is to allow point-to-point interconnection between signal processing chips, and to promote the use of chips from more than one vendor on a single

board.

To permit the use of the Phase 1 chips and Phase 2 chips on the same board, new Phase 1 chips should comply with the Electrical Specification, except that they will utilize a maximum 25 MHz SYSCLK, and the DFNCLK will be operated at 1/4 of the SYSCLK frequency. Since both Phase 1 and Phase 2 chips support a maximum 25 MHz chip I/O at the package edge, this will provide direct interfacing. Redesigned original Phase 1 chips are expected to meet this specification also. This is being done to insure that chips which use the name "VHSIC" will enhance rather than detract from the "-ilities" of future DoD systems.

For existing printed circuit boards, the maximum I/O rate presently supported is 25 MHz. This limit is imposed by the physics of the board level interconnects. In the future, if impedance tuned lines are used, higher I/O rates will be available. Both Honeywell and IBM have demonstrated that 50 MHz communications are available between ICs with impedance controlled lines on a multichip carrier. In addition, the Laser Pantography effort at Lawrence Livermore National Laboratory has constructed "Silicon PC Boards" with propagation velocities of 23 cm/ns as part of their VHSIC Phase 3 effort.

(b) The PI-Bus (Parallel Interface Bus) (Version 2.2, 15 March 1988) specifies the backplane parallel interconnection between VHSIC-based subsystem boards. Unlike microcomputer busses such as the VME or MultiBus, the Pi-Bus has no separate set of lines for addresses. This bus is meant to be a communications medium for systems to exchange messages or buffers of information, and not for retrieving individual words from a memory. All three VHSIC Phase 2 contractors have chosen to implement a 16-bit error detection form of the BIU as a PI-Bus interface for their demonstration modules. IBM has over 1200 fully tested chips available. Honeywell has at least one fully functional part, and has packaged parts undergoing life testing, while the TRW parts are due to be delivered to the Navy in March 1989. The bipolar drivers for the backplane are now available on the commercial market from Signetics. The PI-Bus is a standard interface on the Air Force Common Signal Processor (CSP) and called out in SDI technology programs. It has been chosen by the Joint Integrated Avionics Working Group (JIAWG) as the backplane control bus for the ATA/ATF/ATH common avionics package. They will use a 16 bit error correcting version in a dual bus configuration, along with a dual TM-Bus, a MIL-STD-1553B serial bus, and a High Speed Data Bus. The Air Force ATF and the Army ATH (or LHX) are each in the Demonstration/Validation phase with two competing contractors. The Navy ATA has entered full scale development as the A-12. By the ATF/ATA/LHX Commonality Memorandum of Agreement between the Services, the Navy is committed to a P^3I program to use the JIAWG specifications, and all three Services are committed to using the JIAWG avionics specifications/standards in deliveries after 1997. It also should be noted that the SAE-9 HINT committee, which was tasked to define a new parallel backplane bus, has selected the PI-Bus as the candidate for a new standard.

(c) The TM-Bus (Test & Maintenance Bus) (Version 3.0, November 1987) provides a serial backplane interconnection for the same 32 module set serviced by the PI-Bus through four interconnect lines: Clock, Master Data, Control, and Slave Data.

The TM-Bus will be used by the Phase 2 VHSIC contractors on their demonstration brassboards. In addition, it is being quoted as the maintenance interface for several VHSIC contractors insertion efforts, and will be used by the ATA/ATF/ATH as explained in the PI-Bus section. The TM-Bus is being incorporated into draft standard IEEE 1149.X. Members of the IEEE Test Technology Committee working on this include Chuck Hudson (Honeywell), Jim Becker (IBM), and Pat McHugh (Army), who are also part of the VHSIC test bus effort.

(d) The ETM-Bus (Element Test & Maintenance Bus) (Version 3.0, November 1987) contains the electrical and protocol definitions for a synchronous serial bus. This standard allows the designer to use chips from various VHSIC manufacturers on the same board and connect them to a common maintenance controller, which in turn receives its control and instructions via a backplane TM-Bus. A single controller could thus be used to test a board in both field and depot maintenance operations.

In its present configuration, the ETM bus is quite similar to the IEEE P1149.1 (JTAG) working group's proposed standard test bus. The principal differences are:

1) The P1149.1 combines the ETM "mode" and "select" lines on a single pin which necessitates a more complicated set of P1149.1 protocols.

2) The P1149.1 treats "boundary scan" as a special case and requires the boundary latches to be excluded from boundary scan.

3) The ETM-Bus includes an extra interface line to allow the part being tested to raise an interrupt to get the Test Controller's attention. This allows self test to proceed asynchronously for very complicated integrated circuits.

4) The P1149.1 does not require parity, nor does it control the number of bits in the command register.

5) The P1149.1 specifically allows an optional device ID register. This, when used, will allow the external tester to ascertain if the correct IC has been inserted.

Several current developmental efforts on fault tolerant signal and data processors are designing this interface into their systems.

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Radiation Hardening

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Qualification, Reliability and Test

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Interoperability Specifications

The following specifications are contained in an Army technical report, SLCET-TR-85-0367-8, "VHSIC Phase 2 Submicrometer Technology Development -- Interoperability Standards", dated November 1988. For availability, contact Arnold Bard, Army LABCOM, SLCET, Fort Monmouth, NJ 07703, (201) 544-4469.

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APPENDIX B - CONFERENCES AND WORKSHOPS (1988-1989)

1988 Conferences and Workshops

- VHSIC TECH-FAIR II (Advanced Hands-on Applications Workshop), co-sponsored by the DoD VHSIC Program Office, the Defense Systems Management College, and the Applied Physics Laboratory, held at the Johns Hopkins University Applied Physics Laboratory, MD, June 28-30, 1988

- VHDL Users Group meeting, held at 1988 IEEE Design Automation Conference.

- VHDL Users Group meeting, held in Redondo Beach, CA on October 23-26, 1988.

- Engineering Information System (EIS) Workshop, held in Baltimore, MD on November 14-18, 1988. For information, contact LT Nicholas Naclario, AFWAL/ETED, Wright-Patterson Air Force Base, OH 45433-6543 (513) 255-8647.

- 1988 VHSIC/VLSI Qualification, Reliability, and Logistics Workshop, sponsored by the DoD VHSIC Qualification Committee, held in Scottsdale, AZ on September 27-29, 1988

1989 Conferences and Workshops

- VHDL Users Group Meeting, to be held in Washington, DC in March 1989. For information, contact Randolph Harr, CAD Specialist, 127 Beaumont Avenue, San Francisco, CA 94118, (415) 387-8262.

- Advanced Microelectronics Technology Qualification, Reliability, and Logistics Workshop, to be held in Albuquerque, NM, August 29-31, 1989. For information, contact Edward B. Hakim, Army ETDL, (201) 544-2185.

- Tri-Service Packaging/Interconnections Conference, to be held in Ft. Monmouth, NJ area in May 1989. For information, contact Owen Layden, Army ETDL, (201) 544-2378.

APPENDIX C - VHSIC POINTS OF CONTACT - GOVERNMENT

DoD Program Office

VHSIC Program Director	Dr. John M. MacCallum	202-693-2978
Deputy Program Director	E. C. Urban	202-697-4198
Deputy Program Director	Dr. S. E. Turnbach	202-697-4198
Technology Security/Insertion	D. G. Hayman	202-697-4198

Army Program Office

Program Director	Dr. C. G. Thornton	201-544-2541
Deputy Program Director	H. Borkan	201-544-2583
Program Manager	R. H. Sproat	201-544-3172

Navy Program Office

Program Director	LCDR P. Gariano, Jr.	202-692-3966
Deputy Program Director	J .P. Letellier	202-767-2937

Air Force Program Office

Program Director	W. J. Edwards	513-255-2911
Program Manager	R. M. Werner	513-255-7142

VHSIC System Design Experts

Communications		
A. Lukosevicius	Army CECOM	201-544-4133
R. Peterson	Navy NOSC	619-553-1164
Electro-Optics		
J. Pupich	Army CECOM	703-664-5207
Electronic Warfare		
J. Cervini	Army CECOM	201-544-3224
Radar/Sonar		
V. Organic	Army PM RADAR	201-544-5111
J. P. Letellier	Navy NRL	202-767-2937

P. Reimel	Navy NADC	215-441-1933
D. Mukai	AF AFWAL/AARM	513-255-5359

Signal Processing

K. Bromley	Navy NOSC	619-553-2353
J. P. Letellier	Navy NRL	202-767-2937
J. Holtkamp	Navy NAC	317-353-3249

VHSIC Issue Experts

Built-In-Test/Design for Test

W. Debany	AF RADC	315-330-2047
P. McHugh	Army LABCOM	201-544-3501
M. Vineberg	Navy NOSC	619-553-4957

Design Automation/VHDL/ADAS

C. Bosco	Army LABCOM	201-544-2912
D. Rooney	Navy NRL	202-767-2937
J. Hines	AF AFWAL	513-255-4448

Interoperability

A. Bard	Army LABCOM	201-544-4469
J. P. Letellier	Navy NRL	202-767-2937

Packaging

O. Layden	Army LABCOM	201-544-2378
P. Speicher	AF RADC	315-330-4055
D. McKee	Navy NOSC	619-553-5396

Radiation Hardening

J. M. McGarrity	Army HDL	301-394-3180

Qualification: Line Certification, Procedure, Specifications

M. Adams	DESC EQM	513-296-6258
T. Creek	DESC ECS	513-296-6023

TISSS

W. Russell	AF RADC	315-330-2151
R. Stegmaier	AF RADC	315-330-3989

VHSIC Definition

T. Creek	DESC ECS	513-296-6023
S. Turnbach	DoD CET	202-697-4198

APPENDIX D - VHSIC POINTS OF CONTACT - CONTRACTS

	Contractor	DoD
TECHNOLOGY INSERTION		
Enhanced PLRS User Unit Hughes Aircraft Company Contracts: DAAB07-84-C-K588 DAAB07-82-C-J096	Larry Hersey 714-441-9981	Albert Lukosevicius Army CECOM 201-544-4133
LHX Mission Computer Boeing/Sikorsky Contract DAAJ02-86-C-0016	D. Tinkham 316-526-3717	G. Tomlin Army AVSCOM 314-263-1810
LHX Mission Computer McDonnell Douglas/Bell Helicopter Contract DAAJ02-86-C-0017	R. Webb 602-891-7890	G. Tomlin Army AVSCOM 314-263-1810
TOW VHSIC Automatic Target Tracker Texas Instruments Contracts: DAAH01-85-C-1161 (MICOM) MDA972-88-C-0052 (DARPA)	Ken Byrn 214-480-1046	R. Mitchell Army MICOM 205-876-3672
Firefinder VHSIC Technology Insertion Demonstration Hughes Aircraft Company Contract DAAK20-84-C-0433	Nathan Newton 714-732-2300	Vincent Organic Army LABCOM 201-544-5111
Combat Vehicle VHSIC Integrated System (CVIS) Westinghouse Contract DAAA21-87-C-0281	J. McKindles 301-765-7777	Larry Yung Army ARDEC 201-724-7051
Combat Vehicle VHSIC Integated System (CVIS) General Dynamics Contract DAAA21-87-C-0287	Paul Hedtke 619-547-3787	Larry Yung Army ARDEC 201-724-7051
MEDFLI-VTAM ESL Corporation Contract DAAK20-85-C-0648	D. Klaus 408-743-6455	John Cervini Army CECOM 201-544-3224
MEDFLI-VMASS General Electric Corporation Contract DAAB07-87-C-P040	J. Springer 609-338-3505	Patrick McHugh Army CECOM 201-544-4019

Hellfire IIR Seeker Ford Aerospace and Communications Contract DAAH01-85-C-A138	B. Vin 714-720-7118	Ted Peacher Army MICOM 205-876-3484 Albert Bramble Army LABCOM 201-544-3175
Hellfire IIR Seeker Texas Instruments Contract DAAH01-85-C-A118	W. Sullivan 214-462-4872	Ted Peacher Army MICOM 205-876-3484
Hellfire PA/VHSIC Chip Integration McDonnell Douglas Contract DAAH01-85-C-A104	D.M. Karnes 714-986-2176	Ted Peacher Army MICOM 205-876-3484
Multirole Survivable Radar Raytheon Contract DAAH01-85-C-A034	L. Gallerani 617-274-3728	Tilden Tippit Army MICOM 205-876-1707
Multirole Survivable Radar (MRSR) Westinghouse Contract DAAH01-85-C-A033	G. Hays 301-765-2114	Tilden Tippit Army MICOM 205-876-1707
Army Command and Control System (ACCS) TRW Contract DAAB07-88-C-A006	K. Szeto 213-814-1787	J. Vacquez Army CECOM 201-544-3600
Enhanced Modular Signal Processor (EMSP) AT&T/Honeywell Contract N00024-81-C-7318	L. Hooker 919-279-4740	David Howard Navy NAVSEA 202-746-0581
MK50 Advanced Lightweight Torpedo Honeywell Contract N00024-83-C-6254	S. Sivan 612-931-6995	Tim Singleton Navy NAVSEA 202-692-0637
HF/EHF VHSIC Terminal Brassboard (VTB) TRW Contract N00039-81-C-0414	C.M. Thomas 213-814-2237	Keene Taylor Navy SPAWAR 202-951-2188
AN/AYK-14(V) Standard Airborne Computer CDC/Unisys Contract N00019-86-C-0002	Richard Balestra 301-468-8183	Bruce Anderson Navy NAVAIR 202-692-3298

VHSIC Communications Processor (VCP) TRW Contract N00019-82-C-0330	A. Schmitt 619-592-3472	Thomas Schlegel Navy NAVAIR 202-692-2514
Combat Direction Finder Sanders Associates Contract: classified	J. Eacobacci 603-885-5875	G. Woodward Navy SPAWAR 202-692-2395
Advanced Onboard Signal Processor IBM Contract F30602-86-C-0151	R. Kettlekamp 703-367-3930	F. Schmandt AF RADC 315-330-3091
Advanced Onboard Signal Processor TRW Contract F30602-86-C-0150	E. Yang 213-536-1431	F. Schmandt AF RADC 315-330-3091
Cruise Missile Advanced Guidance (CMAG) General Dynamics F33615-84-C-1460 Honeywell F33615-84-C-1500	Paul Hedtke 619-547-3787 David Nielsen 612-541-2482	E. Hamilton AFWAL 513-255-2713 Darrell Barker 513-255-8639
Common Signal Processor (CSP) IBM Contract F33615-84-C-1470	Robert Estrada 703-367-4279	Dale Van Cleave AFWAL 513-255-7708
VHSIC Avionics Modular Peocessor (VAMP) (Formerly MIL-STD 1750A Computer) Westinghouse Contract F33615-84-C-1465	David Sartorio 301-765-6744	G. Konomos AFWAL 513-255-3765
Speech Enhancement Unit Martin-Marietta Contract F30602-85-C-0266	John Damoulakis 301-787-2880	M. Mayner AF RADC 315-330-4587
MILSTAR Terminal/Modem Processor TRW Contract N00039-81-C-0414	C.M. Thomas 213-536-3104	Stuart Talbot AF RADC 315-330-3091
F-15 Central Computer IBM under subcontract to McDonnell Douglas Contract F33657-84-C-2228, POE7E358	J. Davey (IBM) 607-751-3535 W. Russell (McDonnell-Douglas) 314-223-7468	R. Anderson AF ASD 912-926-2826

F-16 APG-68/Radar VHSIC Programmable Signal Processor (VPSP) Westinghouse Contract F33657-81-C-0115	David Sartorio 301-765-6744	David DeMoss AFSC 513-255-8944
E-3A Signal Processor Westinghouse Contract F30602-86-C-0221	David Sartorio 301-765-6744	AF ESD
VHSIC TTL Gate Array Honeywell Contract F04606-86-C-0813	David Wick 719-540-3580	Theodore Glum AF SM-ALC 916-643-6454
Logistics Retrofit Engineering 1750A Electronic Module General Dynamics Contract F04606-87-D-0034	T. Williams 916-920-3663	Theodore Glum AF SM-ALC 916-643-6454
Generic VHSIC Spaceborne Computer (GVSC) IBM Contract F29601-87-C-0006	Robert Estrada 703-367-4279	R. Herndon AF 505-846-0855
Generic VHSIC Spaceborne Computer (GVSC) Honeywell Contract F29601-87-C-0018	David Wick 719-540-3580	R. Herndon AF 505-846-0855

PHASE 1

Honeywell - Solid State Electronics Division Contract F33615-81-C-1527	R. Julkowski 612-541-2066	Guy Couturier AFWAL 513-255-8667
Hughes Aircraft - Industrial Electronic Group Contract DAAK20-81-C-0383	Robert Stone 619-931-5182 Ronald Dodge 619-931-3196	Albert Bramble Army LABCOM 201-544-3175
IBM - Federal Systems Division Contract N00029-81-C-0416	Robert Estrada 703-367-4279	LCDR Patrick Gariano Navy SPAWAR 202-692-3966
Texas Instruments - Equipment Group Contract DAAK20-81-C-03822	J. Wilson 214-995-2395	Robert Sproat Army LABCOM 201-544-3172

TRW - Military Electronics Division Motorola Contract N00039-81-C-0414	Tom Zimmerman 213-814-2400 E. Daniels 602-897-3572	LCDR Patrick Gariano Navy SPAWAR 202-692-3966
Westinghouse - Advanced Technology Lab National Semiconductor Contract F33615-81-C-1532	David Sartorio 301-765-6744 Jerry Streb 408-721-5448	Guy Couturier AFWAL 513-255-8667

QUALIFICATION

VHSIC Gate Array Qualification Westinghouse Contract F33615-81-C-1532	Richard Lyman 301-765-2379	Kevin A. Kwiat AF RADC 315-330-2047

PHASE 2

Honeywell - Solid State Electronics Division Contract F33615-84-C-1500	David Nielsen 612-541-2482	Darrell Barker AFWAL 513-255-8634
IBM - Federal System Division Contract DAAK20-85-C-0376	Robert Estrada 703-367-4279 Philip Johnson 703-367-5547	Robert Sproat Army LABCOM 201-544-3172
TRW - Military Electronics Division Motorola Contract N00039-85-C-0111	Tom Zimmerman 213-814-2400 Charles Meyers 512-928-6940	LCDR Patrick Gariano Navy SPAWAR 202-692-3966

PHASE 3 - DESIGN TOOLS / IDAS

VHDL Design Workbench Vista Technologies Contract DAAL01-85-C-0435	S. Swamy 312-593-8686	Charles Bosco Army LABCOM 201-544-2912
VHSIC Hardware Descript Language (VHDL) Intermetrics Contract F33615-83-C-1003	V. Berman 301-657-3775	John Hines AFWAL 513-255-4448

VHDL Independent Validation and Verification United Technologies Microelectronics Center Contract F33615-85-C-1760	J. Costentino 303-594-8237	John Hines AFWAL 513-255-4448
Processor Synthesis Tool for VHDL Honeywell Computer Science Lab Contract F33615-85-C-1261	S. Krolikosky 612-887-5701	John Hines AFWAL 513-255-4448
VHSIC Silicon Compiler Research Triangle Institute Contract F33615-85-C-1863	James Clary 919-541-6951 G. Frank	John Hines AFWAL 513-255-4448
Interface Between CMOS Process and Silicon Compiler National Semiconductor Corp Contract F33615-85-C-1867	Jerry Streb 408-721-5448	John Hines AFWAL 513-255-4448
Support To IEEE VHDL Standardization CAD Language Systems, Inc. Contract F33615-86-C-1050	M. Shahdad 301-424-9445	John Hines AFWAL 513-255-4448
Joint US/Canadian VHDL Rehost Bell Northern Research / Intermetrics Contract F33615-87-C-1463 (U. S. participation)	D. Agnew (BNR) 613-726-4615 V. Berman (Intermetrics) 301-657-3775	John Hines AFWAL 513-255-4448
ADAS Integration into VHDL Support Environment Research Triangle Institute Contract N00039-86-C-0057	James Clary 919-541-6951	Paul Hunter Navy NRL 202-767-3517
Annotation Language for VHDL Stanford Center for Integrated Systems Contract F33615-86-C-1137	Youm Huh 415-723-1852 David Luckham 415-723-1242	John Hines AFWAL 513-255-448
Enhanced AMSDS JRS Research Laboratories Contract N00039-87-C-0256	Erwin Warshawsky 714-974-2201	Helmut Roth Navy NSWC 301-394-1480
System Level Tools for the ADAM System U. of Southern California Contract N00039-87-C-0194	Alice Parker 213-743-5560	Vernon Anderson Navy NWC 619-939-3100

Hierarchical Design for Testability Research Triangle Institute/ University of Virginia Contract DAAL01-86-C-0039	James Clary 919-541-6951	Charles Bosco Army LABCOM 201-544-2912
Analog Design With VHDL Dartmouth University Contract F33615-87-C-1423	C. Hutchinson 603-646-2238	John Hines AFWAL 513-255-4448
Object-Oriented Chip Design Using VHDL Rensselaer Polytechnic Institute Contract F33615-87-C-1435	E. Rogers 518-276-6909	LT Nick Naclerio AFWAL 513-255-7142
Artificial Intelligence Interface to the ADAS System Research Triangle Institute/OCTY, Inc. Contract DAAL01-86-C-0040	N. Kanopoulos 919-541-7341	C. Bosco 201-544-2912
Engineering Information System Honeywell/CDC/TRW/CAD Language Systems/ McDonnell-Douglas/Arizona State University Contract F33615-87-C-1401	R. Kant 612-782-7322	LT Nick Naclerio 513-255-7142 Vernon Anderson Navy NWC 619-939-3100

PHASE 3 - LITHOGRAPHY

X-Ray Lithography Equipment Perkin Elmer Contract DAAK20-84-C-0378	F. Scott 203-834-6135	J. H. Kwiatkowski Army LABCOM 201-544-3576
X-Ray Lithography Spire Corporation Contract DAAL01-88-C-0807	W. Helgeland 617-275-6000	J. H. Kwiatkowski Army LABCOM 201-544-3576
Advanced Wafer Imaging System (AWIS) GCA Contract DAAL01-85-C-0460	P. Bachman 617-275-9000	Dean Woo Army LABCOM 201-544-4418
Laser Pantography Lawrence Livermore Laboratory National Laboratory Task Assignment	L. Wood B. McWilliams 415-422-7286	J.P. Letellier Navy NRL 202-767-2937

PHASE 3 - RADIATION HARDENING

Radiation Hardened Bulk CMOS Motorola Contract DNA001-84-C-0403	E. Daniels 602-897-3572	LCDR Lewis Cohn DNA 202-325-7016
Radiation Hardened CMOS/SOS General Electric Contract DNA001-84-C-0404	P. Neffeneggar 919-549-3642	LCDR Lewis Cohn DNA 202-325-7016
Radiation Hardened Bulk CMOS Westinghouse/National Semiconductor Contract DNA001-86-C-0134	David Sartorio 301-765-6744	LCDR Lewis Cohn DNA 202-325-7016

PHASE 3 - QUALIFICATION, RELIABILITY, AND TEST

TISSS Independent Validation and Verification Digicomp Contract F30602-86-D-0025	J. Elkens 607-273-5900	W. Russell AF RADC 315-330-2151
Tester Independent Support Software System (TISSS) Harris Corporation Govt. Aerospace Division Contract F30602-84-C-0168	D. Lehtonen 305-729-4025	W. Russell AF RADC 315-330-2151
VHSIC Generic Qualification Procedures GE/ATT/Honeywell Contract F30602-86-C-0172	P. Tracey 315-793-7491	Charles Messenger AF RADC 315-330-3766
Reliability Assessment of Gate Arrays GTE Contract F30602-86-C-0176	J. Meschi 312-681-7100	Mark Gorniak AF RADC 315-330-2047
Non-Destructive Evaluation of Metallurgical Tape Bonds Vanzetti Contract F30602-86-C-0049	A. Traub 617-828-4650	Patricia Speicher AF RADC 315-330-4055
Non-Destructive Package Screening Sonoscan Contract F30602-86-C-0050	L. Kessler 312-766-7088	Patricia Speicher AF RADC 315-330-4055

Reliability Prediction Modeling IIT Research Institute/Honeywell Contract F30602-86-C-0261	W. Denson 315-330-4151 R. Maciolek 612-541-2914	Peter Manno AF RADC 315-330-4635
VHSIC Impact on System Reliability General Dynamics Contract F30602-85-C-0007	S. Gray 817-763-3441	Bruce Dudley AF RADC 315-330-2608
Maintenance Concepts for VHSIC Honeywell Contract F30602-85-C-0091	S. P. Divakaruni 612-782-7433	D. Richards AF RADC 315-330-3476

PHASE 3 - PACKAGING

Multichip Packages Texas Instruments Contract DAAL01-85-C-0442	R. Natali 214-995-4100	Owen Layden Army LABCOM 201-544-2378
Perimeter Chip Carrier Package General Ceramics/Martin Marietta Contract DAAL01-86-C-0001	R. Sisolak 714-630-6108	Owen Layden Army LABCOM 201-544-2378
Tape Automated Bonding (TAB) Honeywell / 3M Contract DAAL01-85-C-0441	R. Maciolak 612-541-2914	Owen Layden Army LABCOM 201-544-2378

APPENDIX E - GLOSSARY OF ACRONYMS AND TECHNICAL TERMS

4PM	Four Port Memory
A-6F	Navy Attack Aircraft
AASP	Advanced Anti-Radiation Missile Signal Processor
ABBM	Acoustic Beamformer Brassboard Module
ACCS	Army Command and Control System
ACE	Array Computing Element
ACS	Array Controller/Sequencer
ADAM	Advanced Design Automation System
ADAS	Architecture Design and Assessment System
ADB	Advanced Digital Bipolar (Honeywell technology)
AEBLE	Advanced Electron Beam Lithography Equipment
AEGIS	Advanced Electronic Guidance and Intercept System
AFIT	Air Force Institute of Technology
AG	Address Generator
AI	Artificial Intelligence
AJ	Anti-Jam or Jam Resistant
ALU	Arithmetic Logic Unit
ALWT	Advanced Lightweight Torpedo (MK-50)
AMAC	Add Multiply Accumulate
AMGS	Automatic Microcode Generation System
AMSDS	Automated Microcode Compiler Synthesis & Design System
AMTE	Automated Microcircuit Test Equipment
AN/ALQ-131	Airborne Pod-Mounted Electronic Countermeasure (ECM)
AN/ALR-56C,-74	Air Force Radars
AN/APG-65	Navy Coherent Multimode Pulse Doppler Radar
AN/APG-68	Airborne Fire Control Radar
AN/AYK-14(V)	Navy Embedded Standard Airborne Computer
AN/BQQ-5	Sonar System
AN/TPQ-36,-37	Artillery Locating Radars (Firefinder)
AN/UYS-1,-2	Navy Standard Signal Processors
AOSP	Advanced Onboard Signal Processor
AP	Arithmetic Processor
APC	Array Processor Controller
APE	Asynchronous Processing Element
APIO	Array Processor Input/Output
APU	Arithmetic Pipeline Unit; Array Processing Unit
ARM	Anti-Radiation Missile
ASP	Advanced Signal Processor
ASW	Antisubmarine Warfare
ATE	Automatic Test Equipment
ATF	Advanced Tactical Fighter
ATR	Automatic (or Aided) Target Recognition

AU	Arithmetic Unit
AV-8B	Marine Vertical Takeoff and Landing (VTOL) Aircraft
AWACS	Airborne Warning and Control System
AWIS	Advanced Wafer Imaging System
Ada	DoD High Order Programming Language
BEOL	Back End of Line
BIST	Built-In Self Test
BIT	Built-In Test
BIU	Bus Interface Unit
BOPS	Billion Operations Per Second
Brassboard	Field Demonstrable Electronic Model
Breadboard	Laboratory Demonstrable Electronic Model
C3I	Command, Control, Communications, and Intelligence
C4	Controlled, Collapsible Chip Connection
CAD	Computer Aided Design
CALMA	Graphics design system marketed by CALMA Corporation
CAM	Content Addressable Memory
CAM	Computer-Assisted Manufacturing
CAVP	Complex Arithmetic Vector Processor
CC-BUS	Chip to Chip Bus
CDP	Configurable Data Path (chip)
CDR	Critical Design Review
CDRL	Contract Data Requirements List
CGA	Configurable Gate Array
CMAC	Complex Multiply Accumulate
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CS	Convolver Superchip
CSP	Common Signal Processor
CSR	Configurable Static RAM
CTTC	Circuit Technology Test Chip (Honeywell)
DAST	Design, Architecture, Software, and Test
DESC	Defense Electronics Supply Center
DF	Direction Finder
DIFAR	Directional Frequency Analysis and Recording
DIU	Device Interface Unit
DNA	Defense Nuclear Agency
DOD	Department of Defense
DPU	Data Processor Unit
DRAM	Dynamic RAM
DSPE	Double Solid Phase Epitaxy
DTIC	Defense Technical Information Center
E-2C	Navy Airborne Warning and Control System (AWACS)
E-3A	SENTRY Air Force AWACS

E-BEAM	Electron-Beam
EA-6B	Navy EW Aircraft
EAR	Export Administration Regulations
EAU	Extended Arithmetic Unit
EAUM	Extended Arithmetic Unit Multiplier
EBL	Electron Beam Lithographic (Machine)
ECCM	Electronic Counter Countermeasures
ECM	Electronic Countermeasure
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHF	Extremely High Frequency
EIS	Engineering Information System
ELINT	Electronic Intelligence
EMC	Electromagnetic Compatibility
EME	Electromagnetic Effects
EMI	Electromagnetic Interference
EMP	Electromagnetic Pulse; Electromagnetic Potential
EMSP	Enhanced Modular Signal Processor
EO	Electro-Optic
EOSP	Electro-Optic Signal Processor
EOSPC	Electro-Optic Signal Processor Controller
EP-3E	Electronic Surveillance Aircraft
EPLRS	Enhanced Position Location Reporting System
EPUU	Enhanced PLRS User Unit
ESD	Electrostatic Discharge
ESM	Electronic Support Measure
ETM-Bus	Element Test and Maintenance Bus
EW	Electronic Warfare
F-14D	Navy Fighter Aircraft
F/A-18	Navy Fighter Attack Aircraft
FAR	Federal Acquisition Regulation
FEOL	Front End of Line
FEP	FLTSAT EHF Package
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FLIR	Forward Looking Infrared
FOG-M	Fiber Optic Guided Missile
FPAP	Floating Point Arithmetic Processor
FSED	Full Scale Engineering Development
FTR	Functional Throughput Rate
Firefinder	Artillery Locating Radars AN/TPQ-36,-37
GBU	General Buffer Unit
GFE	Government Furnished Equipment
GOMAC	Government Microelectronics Applications Conference
GPC	General Purpose Computer
GVSC	Generic VHSIC Spaceborne Computer

HBX	High Brightness X-ray
HDL	Hardware Description Language
HF	High Frequency
HOL	Higher Order Language
HSL	Hierarchical System Language
Hellfire	Anti-Armor Weapon System
I/O	Input/Output
IAC	Information Analysis Center
IAPU	Image Array Processing Unit
IC	Integrated Circuit
ICNIA	Integrated Communication, Navigation, Identification Avionics
IDAS	Integrated Design Automation System
IEEE	Institute of Electrical and Electronics Engineers
IIR	Imaging Infrared
INEWS	Integrated Electronic Warfare System
IPS	Instructions Per Second
IRHVTA	Infra-Red (seeker for) High Value Target Acquisition
IRST	Infrared Search and Track
ISA	Instruction Set Architecture; Imaging Sensor Autoprocessor
ITAR	International Traffic in Arms Regulations
IV&V	Independent Validation and Verification
IVTM	Interconnect Verification Test Module
IVV	Independent Validation and Verification
JEDEC	Joint Electronic Devices Engineering Council
JTIDS	Joint Tactical Information Distribution System
LAMPS	Light Airborne Multipurpose System
LCCC	Leadless Ceramic Chip Carrier
LHX	Light Helicopter Experimental
LOFAR	Low Frequency Analysis and Recording
LP	Laser Pantography
LRE	Logistics Retrofit Engineering Program
LRM	Line Replaceable Module
LSI	Large Scale Integration
M2F2	Multimode Fire and Forget Missile
MAC	Multiplier/Accumulator
MADS	Maintenance And Diagnostics System
MASS	Modular Adaptive Signal Sorter
MC	Micro-Controller
MCC	Multiple Chip Carrier
MCP	Multichip Package
MEDFLI	Miniaturized Electronic Direction Finding Location Indicator
Micrometer	Micron = 10(-6) Meter
Micron	Micrometer = 10(-6) Meter
MIL-STD	Military Standard
MILSTAR	EHF Satellite Communication System

MIPS	Million Instructions Per Second
MK-50	Advanced Light Weight Torpedo (ALWT)
MMG	Multimode Guidance
MMS	Mass Memory Superchip
MMW	Millimeter Wave
MOPS	Million Operations Per Second
MOS	Metal-Oxide Silicon
MOSFET	Metal-Oxide Silicon Field Effect Transistor
MPS	Multipath Switch
MRSR	Multirole Survivable Radar
MS	Matrix Switch
MSI	Medium Scale Integration
MTBF	Mean-Time-Between-Failure; Mean-Time-Between-Fault
MTTR	Mean Time to Repair
NMOS	N-Channel Metal-Oxide Semiconductor
OPS	Operations per Second
OSD	Office of the Secretary of Defense
OUSDA	Office of the Under Secretary of Defense for Acquisition
OUSDRE	Office of the Under Secretary of Defense for Research and Engineering
P3	Naval Patrol Aircraft
P3-C	Navy ASW Aircraft
P3I	Preplanned Product Improvement
Pave Sprinter	Modular Avionics Demonstration Program
PE	Processing Element
PGA	Pin Grid Array
PI-BUS	Parallel Interface Bus (designed during VHSIC-2)
PJH	PLRS/JTIDS Hybrid
PLA	Programmable Logic Array
PLAU	Pipeline Arithmetic Unit
PLRS	Position Location Reporting System
POC	Proof of Concept
PPP	Parallel Pipeline Processor
PRDA	Project Research & Development Announcement
PROM	Programmable Read-Only Memory
PSP	Programmable Signal Processor
PWB	Printed Wiring Board
QCI	Qualification Conformance Inspection
QML	Qualified Manufacturers List
QPL	Qualified Products List
RALU	Register Arithmetic Logic Unit
RAM	Random Access Memory
ROM	Read Only Memory
RPV	Remotely Piloted Vehicle
RTL	Register Transfer Language
RWR	Radar Warning Receiver

S3	Naval Early Warning Aircraft (including radar system)
SCM	Single-Chip Module (used interchangeably with SCP)
SCP	Single-Chip Package (used interchangeably with SCM)
SDI	Strategic Defense Initiative
SECDED	Single Error Correct, Double Error Detect
SEM	Standard Electronic Module
SEP	Standard EHF Pacjage
SEU	Speech Enhancement Unit
SEU	Single-Event Upset
SGEMP	System Generated Electromagnetic Pulse
SH-60B	(Sikorsky) Helicopter Aircraft
SI Chip	System Interface Chip (BIU + FIU)
SLAM	Scanning Laser Acoustic Microscope
SOW	Statement of Work
SP	Signal Processor
SPE	Signal Processing Element
SPEAR	Solid Phase Epitaxy and Regrowth
SPICE	Public Domain Integrated Circuit Simulation Program
SQC/SPC	Statistical Quality & Process Control
SPS	Systolic Processing Superchip
SRAM	Static RAM; Short Range Attack Missile
SSI	Small Scale Integration
STL	Schottky Transistor Logic
STS	Signal Tracking Subsystem
SubACS	Submarine Advanced Combat System
TAB	Tape Automated Bonding
TAM	Threat Association Module
TISSS	Tester Independent Support Software System
TM-BUS	Test and Maintenance Bus
TOW	Tube Launched, Optically Tracked, Wire Guided Missile
TREE	Transient Radiation Effects in Electronics
TTL	Transistor-Transistor Logic
VAG	Vector Address Generator
VALU	Vector Arithmetic/Logic Unit
VAX	DEC 32-Bit Commercial Computer
VBIU	VHSIC Bus Interface Unit
VCB	VHSIC Communications Brassboard
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits
VID	VHSIC Insertion Demonstration for the EMSP
VLM	Very Large Memory
VLSI	Very Large Scale Integration
VPC	Vector Product Calculator
VPO	(DoD) VHSIC Program Office
VPSP	VHSIC Programmable Signal Processor

VSC	VHSIC Signal Conditioner
VTCA	VHSIC Transmit Control Assembly
WAM	Window Addressable Memory
WCL	Wireless Command Link
WSI	Wafer Scale Integration
XSAR	X-ray Step and Repeat Lithographic Machine
YE	Yield Enhancement
YVR	Yield Verification Run